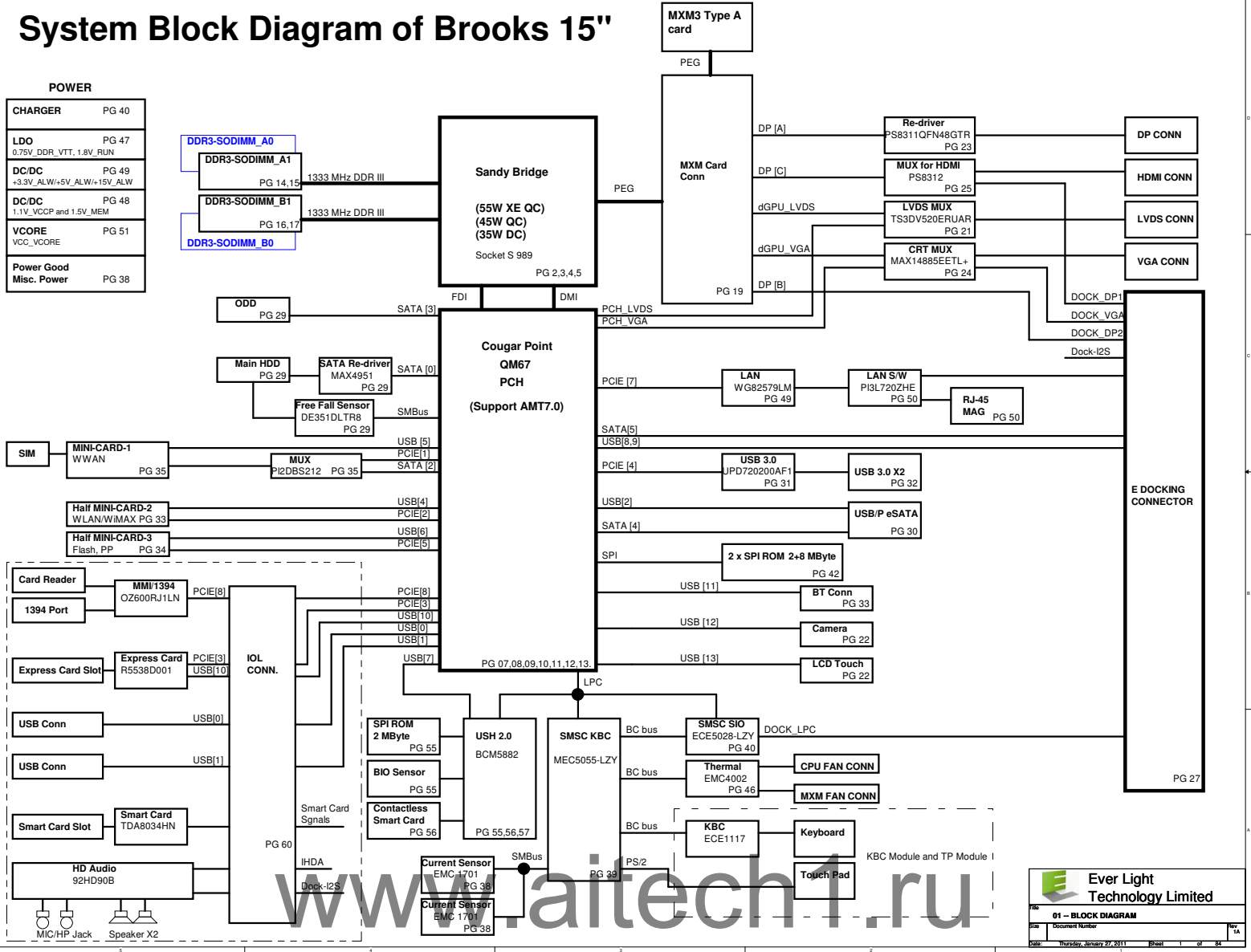
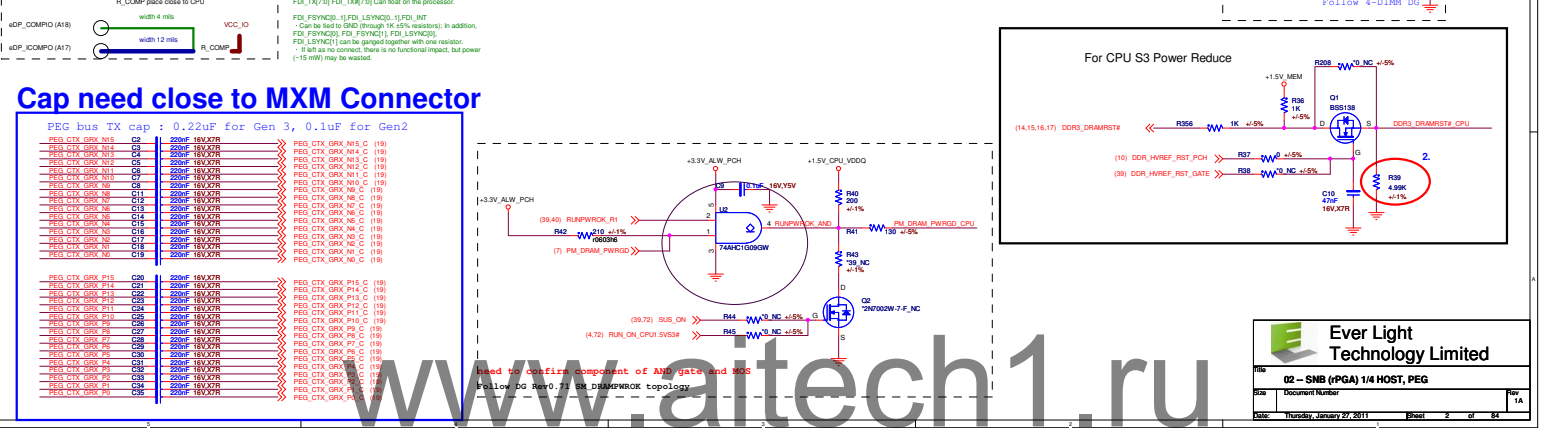
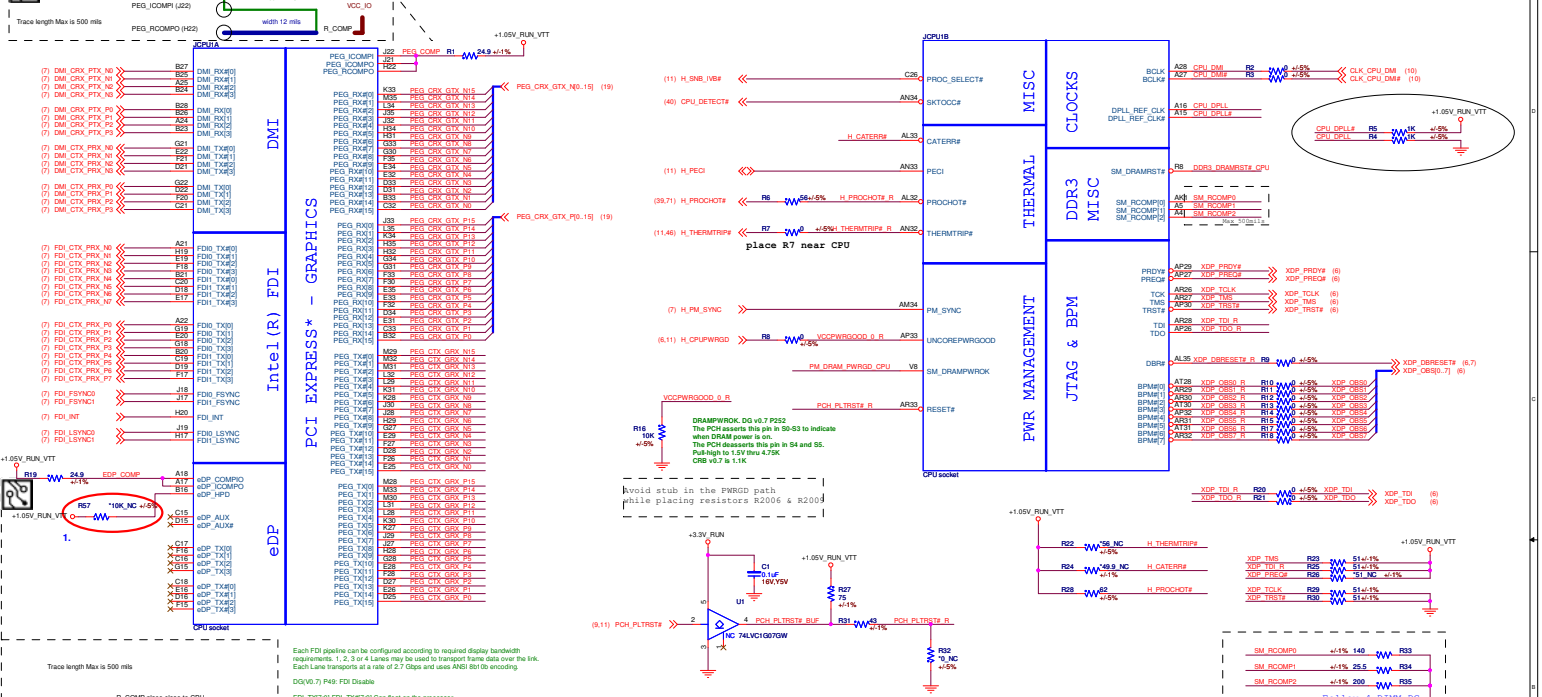


System Block Diagram of Brooks 15"





Cap need close to MXM Connector

PEG bus TX cap : 0.22uF for Gen 3, 0.1uF for Gen2

PEG_CTX_RX_N1	C2	220uF	18VX7R
PEG_CTX_RX_N2	C3	220uF	18VX7R
PEG_CTX_RX_N3	C4	220uF	18VX7R
PEG_CTX_RX_N4	C5	220uF	18VX7R
PEG_CTX_RX_N5	C6	220uF	18VX7R
PEG_CTX_RX_N6	C7	220uF	18VX7R
PEG_CTX_RX_N7	C8	220uF	18VX7R
PEG_CTX_RX_N8	C9	220uF	18VX7R
PEG_CTX_RX_N9	C10	220uF	18VX7R
PEG_CTX_RX_N10	C11	220uF	18VX7R
PEG_CTX_RX_N11	C12	220uF	18VX7R
PEG_CTX_RX_N12	C13	220uF	18VX7R
PEG_CTX_RX_N13	C14	220uF	18VX7R
PEG_CTX_RX_N14	C15	220uF	18VX7R
PEG_CTX_RX_N15	C16	220uF	18VX7R
PEG_CTX_RX_N16	C17	220uF	18VX7R
PEG_CTX_RX_N17	C18	220uF	18VX7R
PEG_CTX_RX_N18	C19	220uF	18VX7R
PEG_CTX_RX_N19	C20	220uF	18VX7R
PEG_CTX_RX_N20	C21	220uF	18VX7R
PEG_CTX_RX_N21	C22	220uF	18VX7R
PEG_CTX_RX_N22	C23	220uF	18VX7R
PEG_CTX_RX_N23	C24	220uF	18VX7R
PEG_CTX_RX_N24	C25	220uF	18VX7R
PEG_CTX_RX_N25	C26	220uF	18VX7R
PEG_CTX_RX_N26	C27	220uF	18VX7R
PEG_CTX_RX_N27	C28	220uF	18VX7R
PEG_CTX_RX_N28	C29	220uF	18VX7R
PEG_CTX_RX_N29	C30	220uF	18VX7R
PEG_CTX_RX_N30	C31	220uF	18VX7R
PEG_CTX_RX_N31	C32	220uF	18VX7R
PEG_CTX_RX_N32	C33	220uF	18VX7R
PEG_CTX_RX_N33	C34	220uF	18VX7R
PEG_CTX_RX_N34	C35	220uF	18VX7R
PEG_CTX_RX_N35	C36	220uF	18VX7R
PEG_CTX_RX_N36	C37	220uF	18VX7R
PEG_CTX_RX_N37	C38	220uF	18VX7R
PEG_CTX_RX_N38	C39	220uF	18VX7R
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PEG_CTX_RX_N40	C41	220uF	18VX7R
PEG_CTX_RX_N41	C42	220uF	18VX7R
PEG_CTX_RX_N42	C43	220uF	18VX7R
PEG_CTX_RX_N43	C44	220uF	18VX7R
PEG_CTX_RX_N44	C45	220uF	18VX7R
PEG_CTX_RX_N45	C46	220uF	18VX7R
PEG_CTX_RX_N46	C47	220uF	18VX7R
PEG_CTX_RX_N47	C48	220uF	18VX7R
PEG_CTX_RX_N48	C49	220uF	18VX7R
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PEG_CTX_RX_N77	C78	220uF	18VX7R
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PEG_CTX_RX_N82	C83	220uF	18VX7R
PEG_CTX_RX_N83	C84	220uF	18VX7R
PEG_CTX_RX_N84	C85	220uF	18VX7R
PEG_CTX_RX_N85	C86	220uF	18VX7R
PEG_CTX_RX_N86	C87	220uF	18VX7R
PEG_CTX_RX_N87	C88	220uF	18VX7R
PEG_CTX_RX_N88	C89	220uF	18VX7R
PEG_CTX_RX_N89	C90	220uF	18VX7R
PEG_CTX_RX_N90	C91	220uF	18VX7R
PEG_CTX_RX_N91	C92	220uF	18VX7R
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PEG_CTX_RX_N96	C97	220uF	18VX7R
PEG_CTX_RX_N97	C98	220uF	18VX7R
PEG_CTX_RX_N98	C99	220uF	18VX7R
PEG_CTX_RX_N99	C100	220uF	18VX7R

For CPU S3 Power Reduce

14.15,16,17) DDR3_DRAMSTK#

14) DDR3_DRAMSTK_RST_PCH

15) DDR3_DRAMSTK_RST_PCH

16) DDR3_DRAMSTK_RST_PCH

17) DDR3_DRAMSTK_RST_PCH

18) DDR3_DRAMSTK_RST_PCH

19) DDR3_DRAMSTK_RST_PCH

20) DDR3_DRAMSTK_RST_PCH

21) DDR3_DRAMSTK_RST_PCH

22) DDR3_DRAMSTK_RST_PCH

23) DDR3_DRAMSTK_RST_PCH

24) DDR3_DRAMSTK_RST_PCH

25) DDR3_DRAMSTK_RST_PCH

26) DDR3_DRAMSTK_RST_PCH

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56) DDR3_DRAMSTK_RST_PCH

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89) DDR3_DRAMSTK_RST_PCH

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100) DDR3_DRAMSTK_RST_PCH

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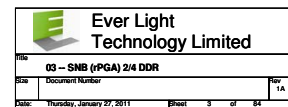
02 - SNG (PGA) 1/4 HOST, PEG

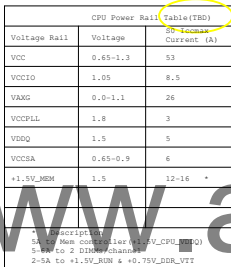
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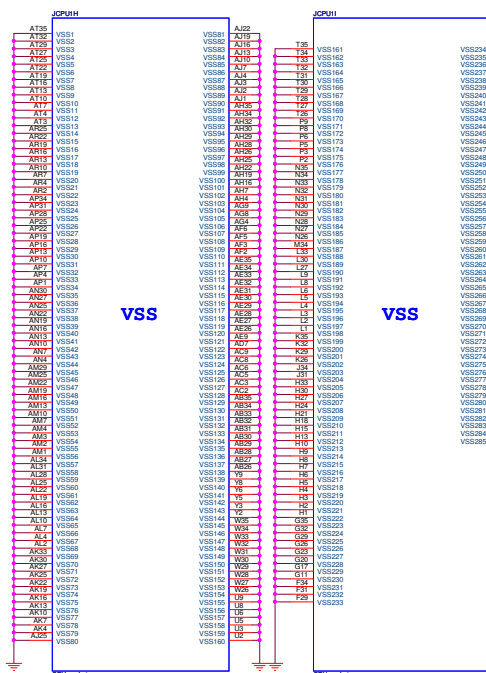
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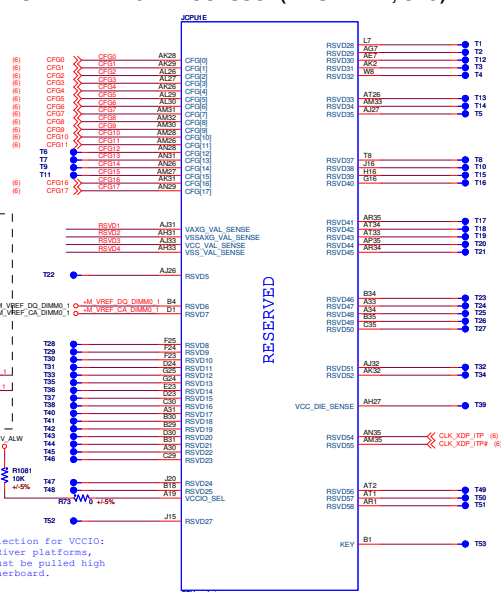




SANDY BRIDGE PROCESSOR (GND)



SANDY BRIDGE PROCESSOR(RESERVED, CFG)



	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 (PEG Defer Training)	PEG Train immediately following xxRESETB deassertion (Default Value)	PEG Wait for BIOS for training

CFG[6:5] (PCIe Port Bifurcation Straps)	11	x16 - Device 1 functions 1 and 2 disable (Default Value)
	10	x8, x8 - Device 1 function 1 enable; function 2 disable
	01	Reserved - (Device 1 function 1 disable; function 2 enable)
	00	x8, x8, x4 - Device 1 function 1 and 2 enable

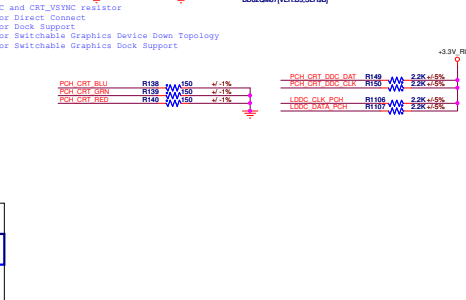
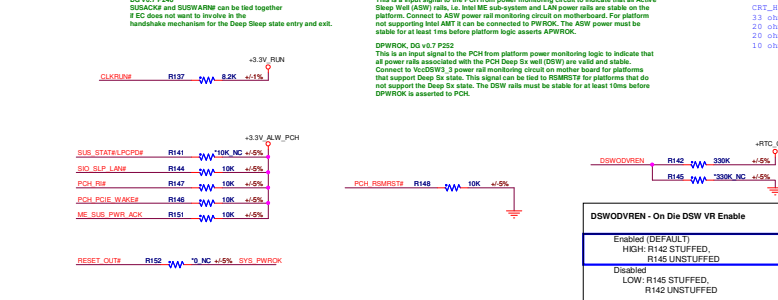
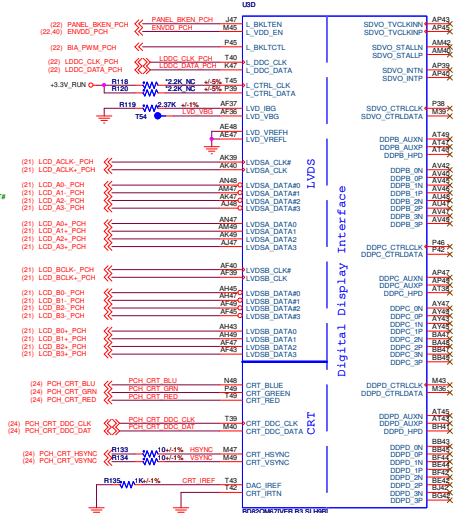
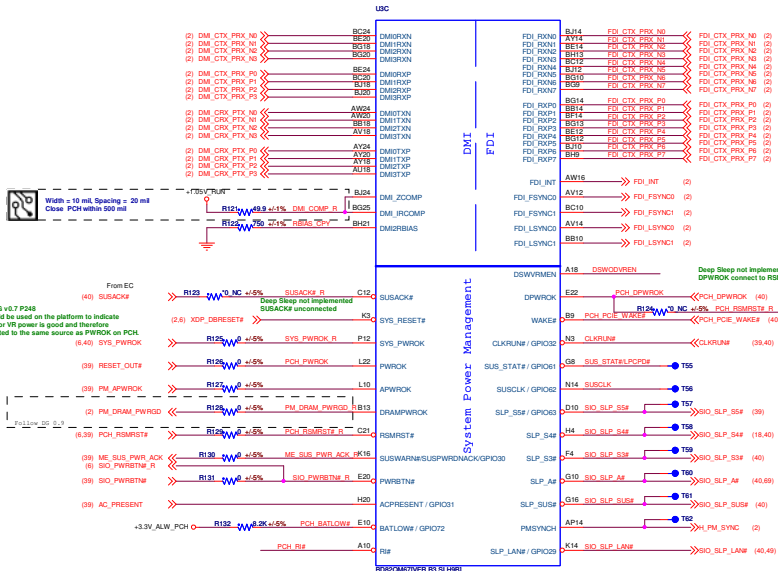


COUGAR POINT (DMI,FDI,GPIO)



PDG v0.7 P166
If the LVDS interface is not implemented,
all signals associated with the interface can
be left as No Connects

COUGAR POINT (LVDS,DDI)



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Cougar Point (PCI,USB,NVRAM)

R191 1K NC $\pm 5\%$ BBS_BTT_R (6,8)
R192 1K NC $\pm 5\%$ BBS_BTT (6,8)

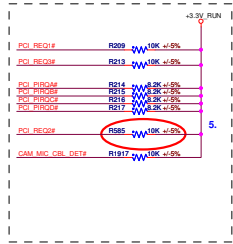
Boot BIOS Strap		
BBS_BTT[1]	BBS_BTT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

GNT3# Strap for ESI mode
This signal has a weak internal pull-up.
Note: The internal pull-up is disabled after PLTRST# deasserts.
Tying this strap low configures DM for ESI compatible operation.
Note: ESI compatible mode is for server platform only.
This signal should not be pulled low for desktop and mobile.

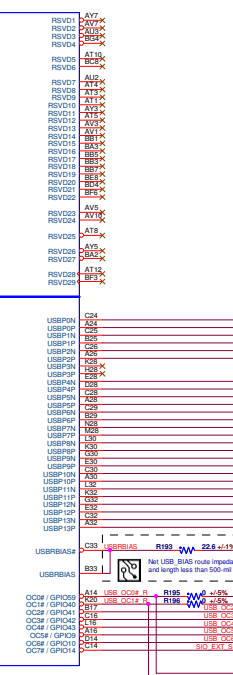
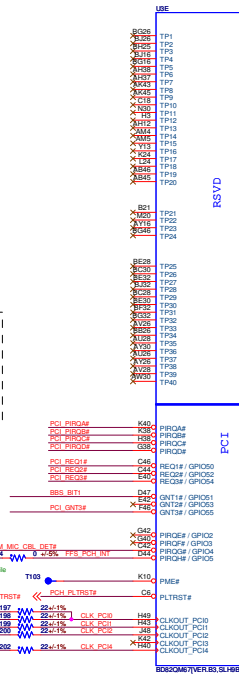
PCI functionality is not available on Mobile

GNT3 functionality is not available on Mobile

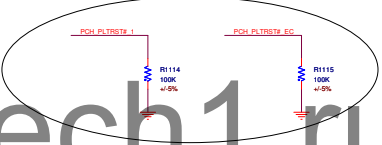
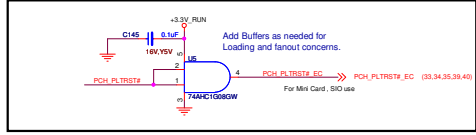
PRQHEq functionality is not available on Mobile



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low - A16 swap override enabled (High - Default)



- Right Side pair top
- Right Side pair bottom
- Back Side
- 2nd Mini Card (WLAN/WIMAX)
- 1st Mini Card (WWAN)
- 3rd Mini Card
- USB
- DOCK
- DOCK
- Express Card
- BlueTooth
- Camera
- LCD Touch

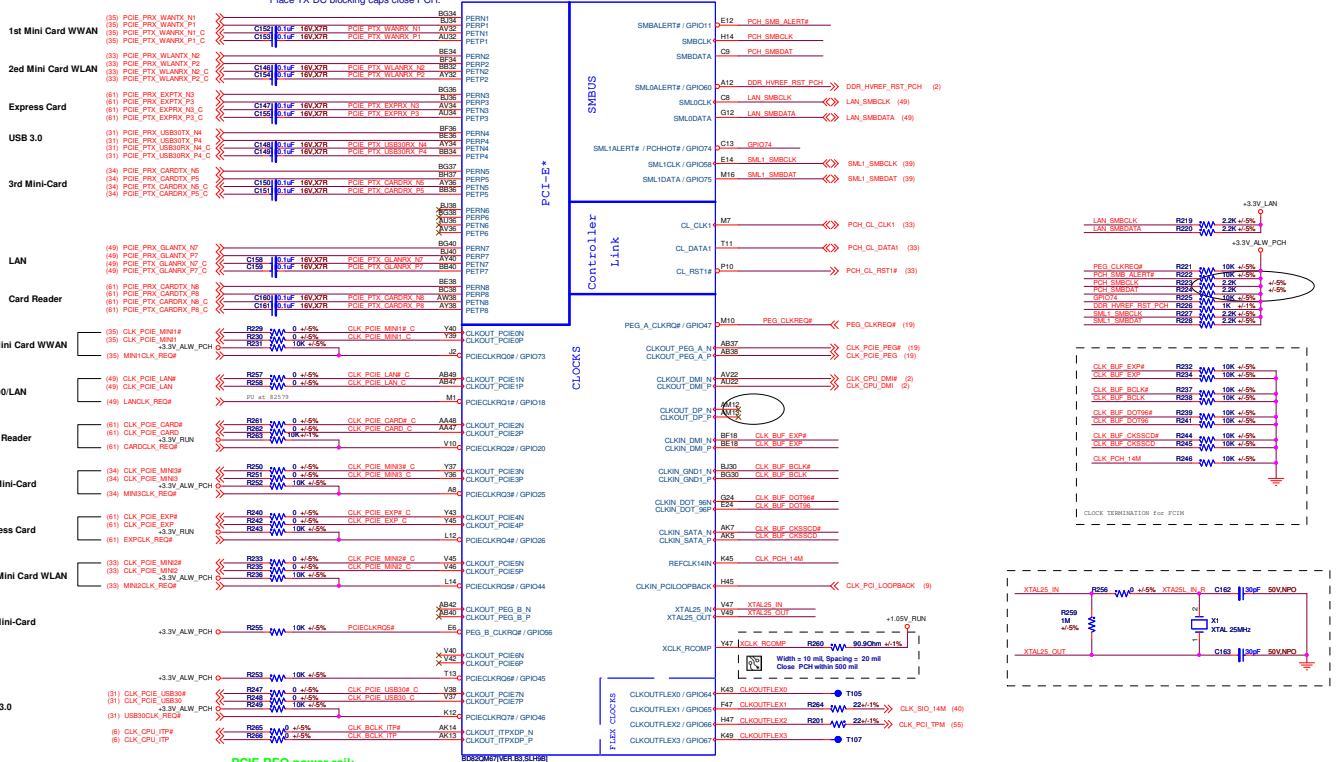




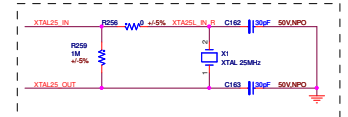
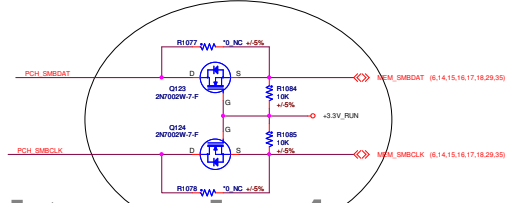
Cougar Point (PCI-E, SMBUS, CLK)

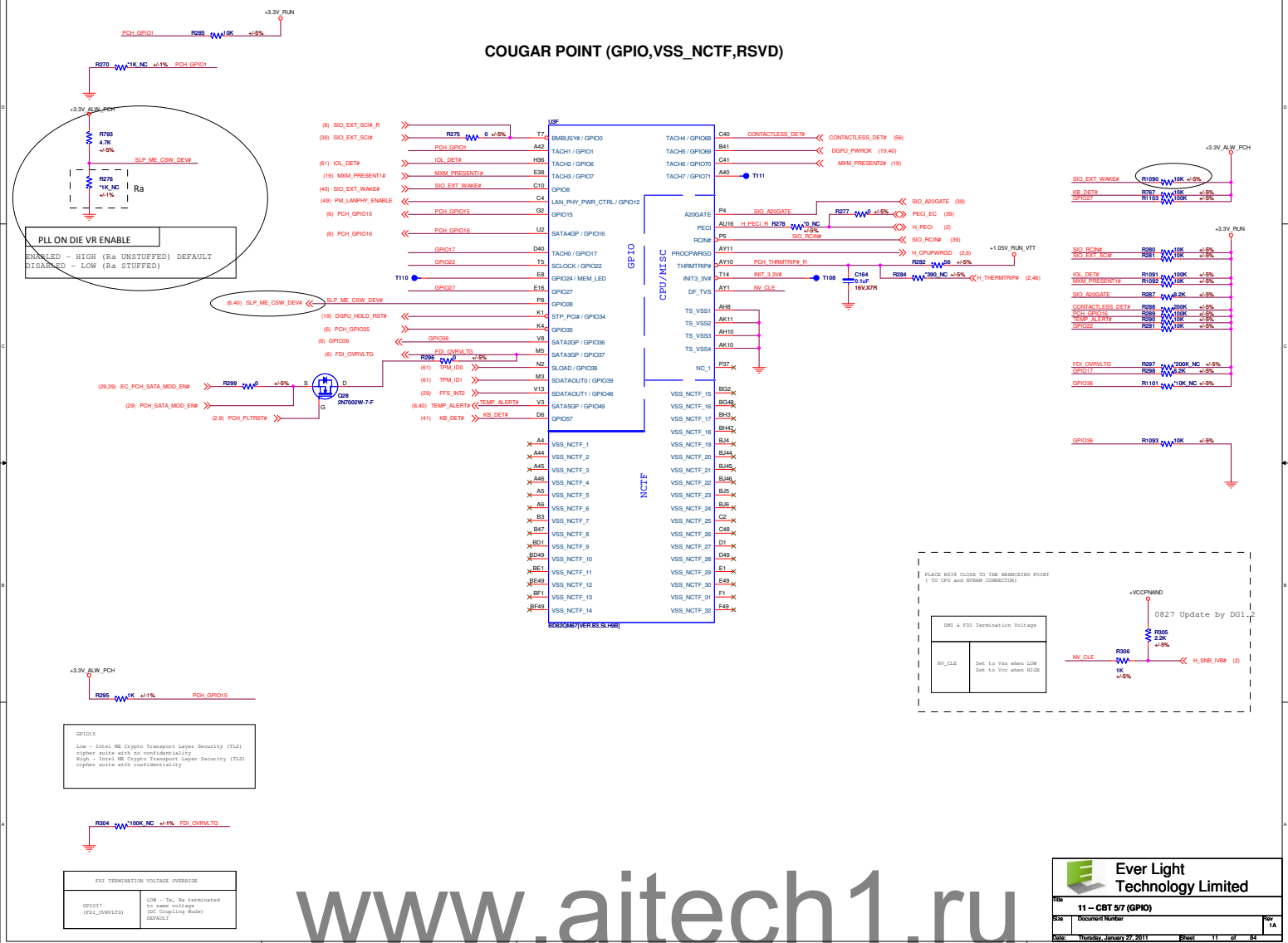
Place TX DC blocking caps close PCH.

USB



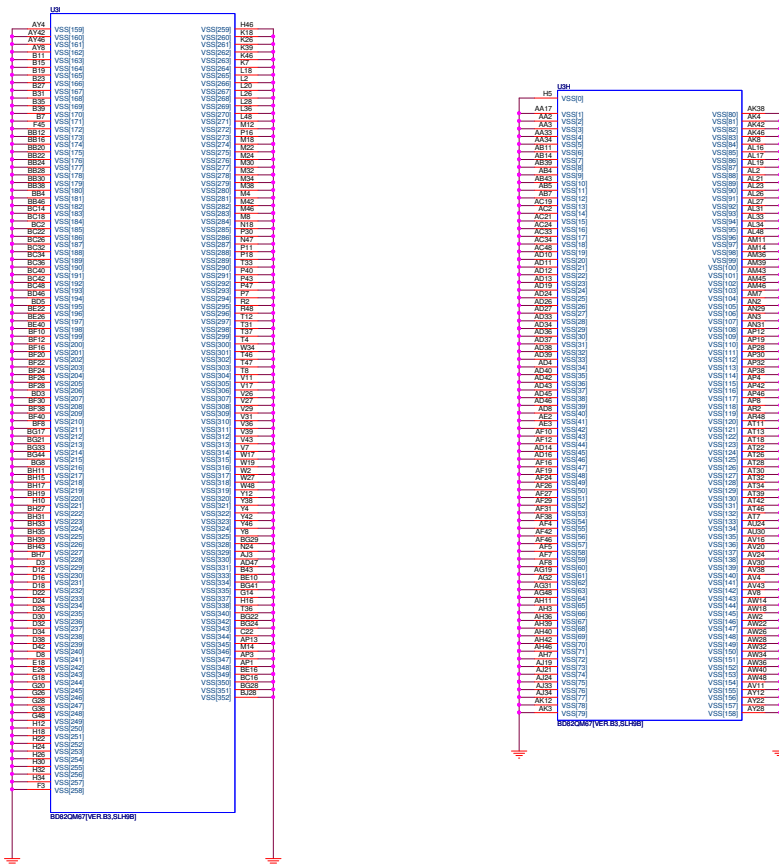
PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2





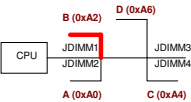


Cougar Point (GND)



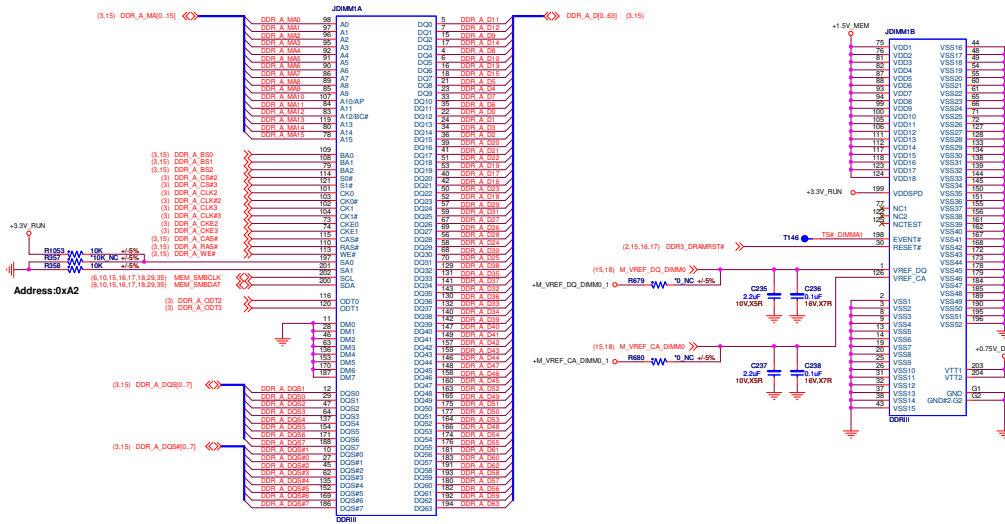
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DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mls	Strobe + 20 mls



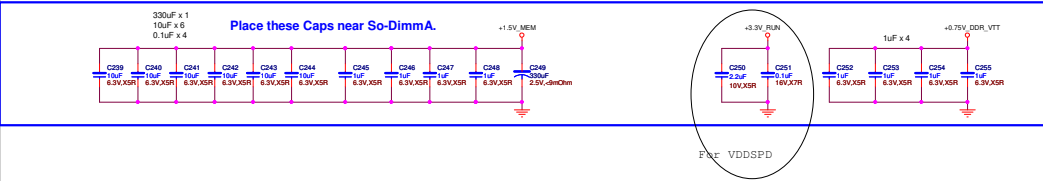
CHA_DIMM1_TOP_SIDE

JDIMM1 is STD type. (H=60)



	SA1	SA0
CHAD	0	0
CHAT	0	1
CHBO	1	0
CHBT	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMC. Clock and Control signals. These capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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15 – SODIMM-204P-A1

Document Number

Thursday, January 27, 2011

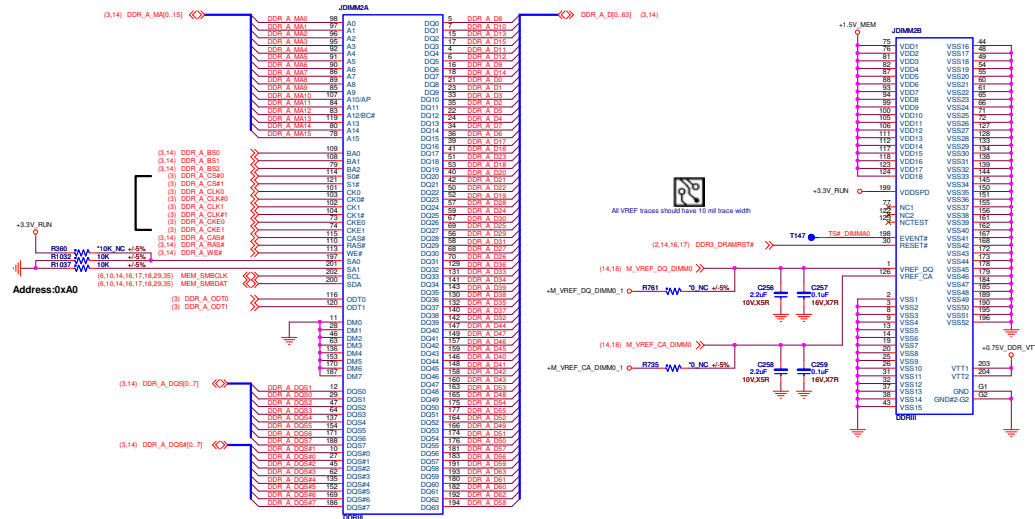
Sheet 14 of 84

Rev A

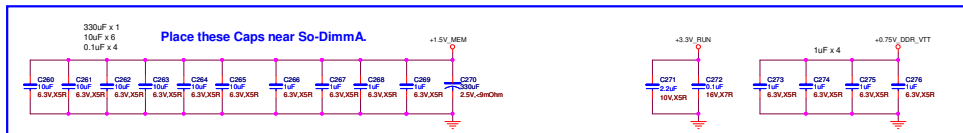
CHA_DIMM0_BOT_SIDE

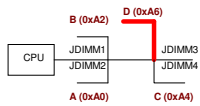
JDIMM2 is RVS type.(H=60)

Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



 +1.5V_{SUS} decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



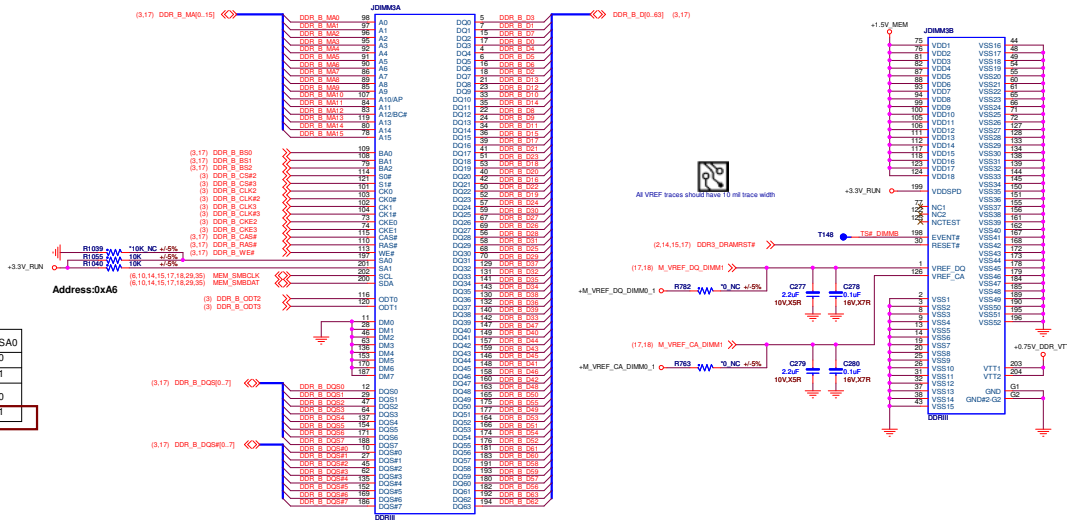


CHB_DIMM1_TOP_SIDE

JDIMM3 is STD type.

DDR3 Length Matching Formulas

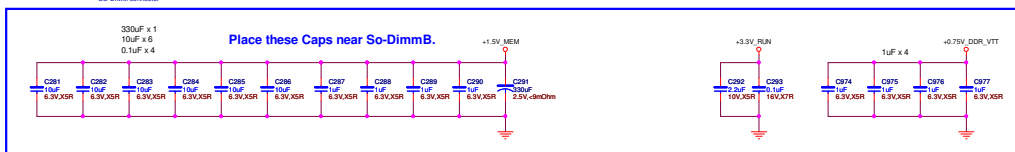
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



	SA1	SA0
CH40	0	0
CH41	0	1
CHB0	1	0
CHB1	1	1



+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals. These capacitors should be placed on the same side of the motherboard as the SO-DIMM connector.



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File: 17 - SODIMM-204P-B0

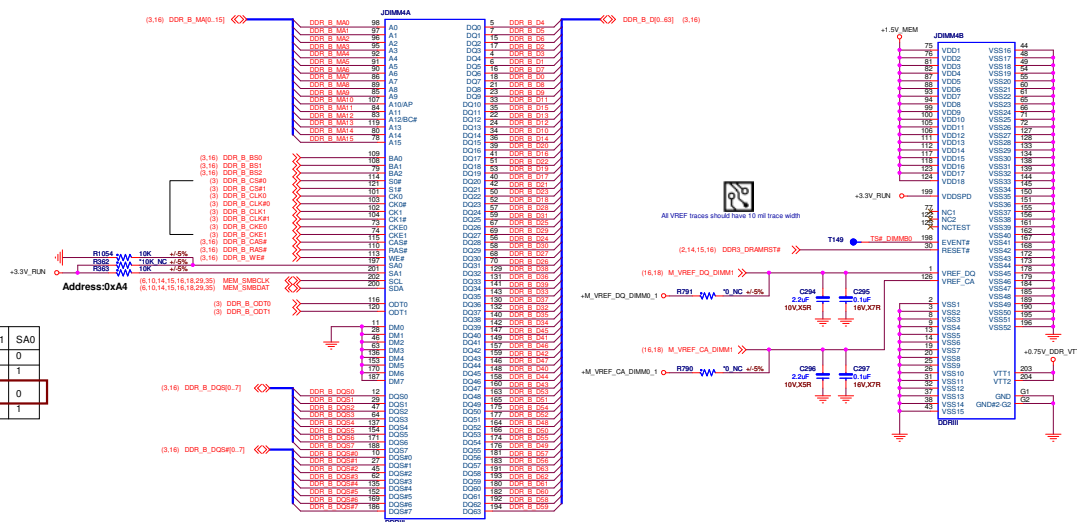
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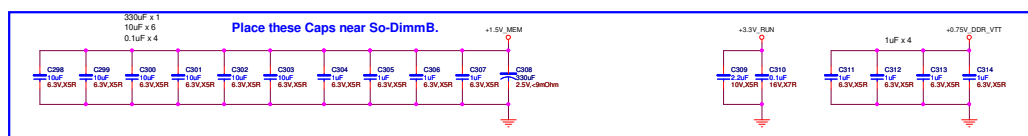
Page: 16 of 24

CHB_DIMM0_BOT_SIDE

JDIMM4 is STD type.



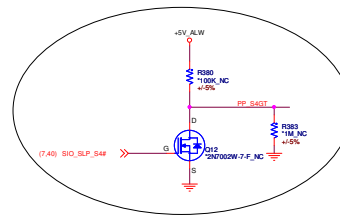
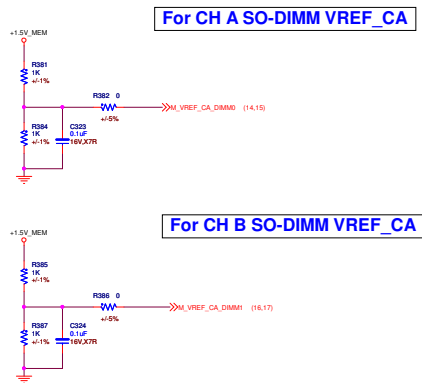
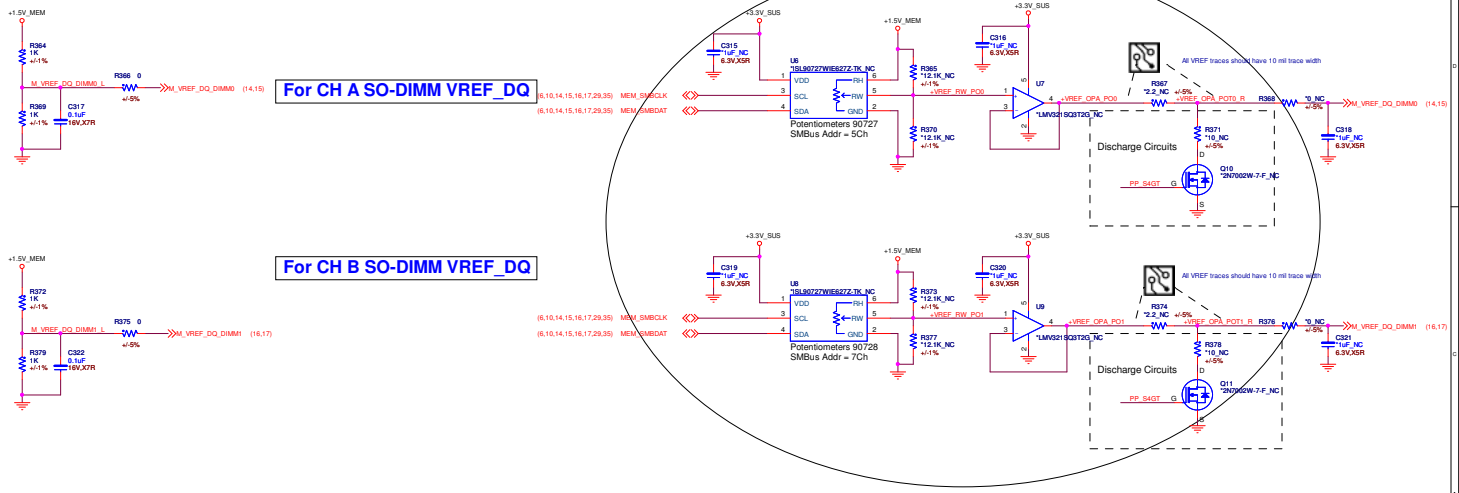
+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector.



Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

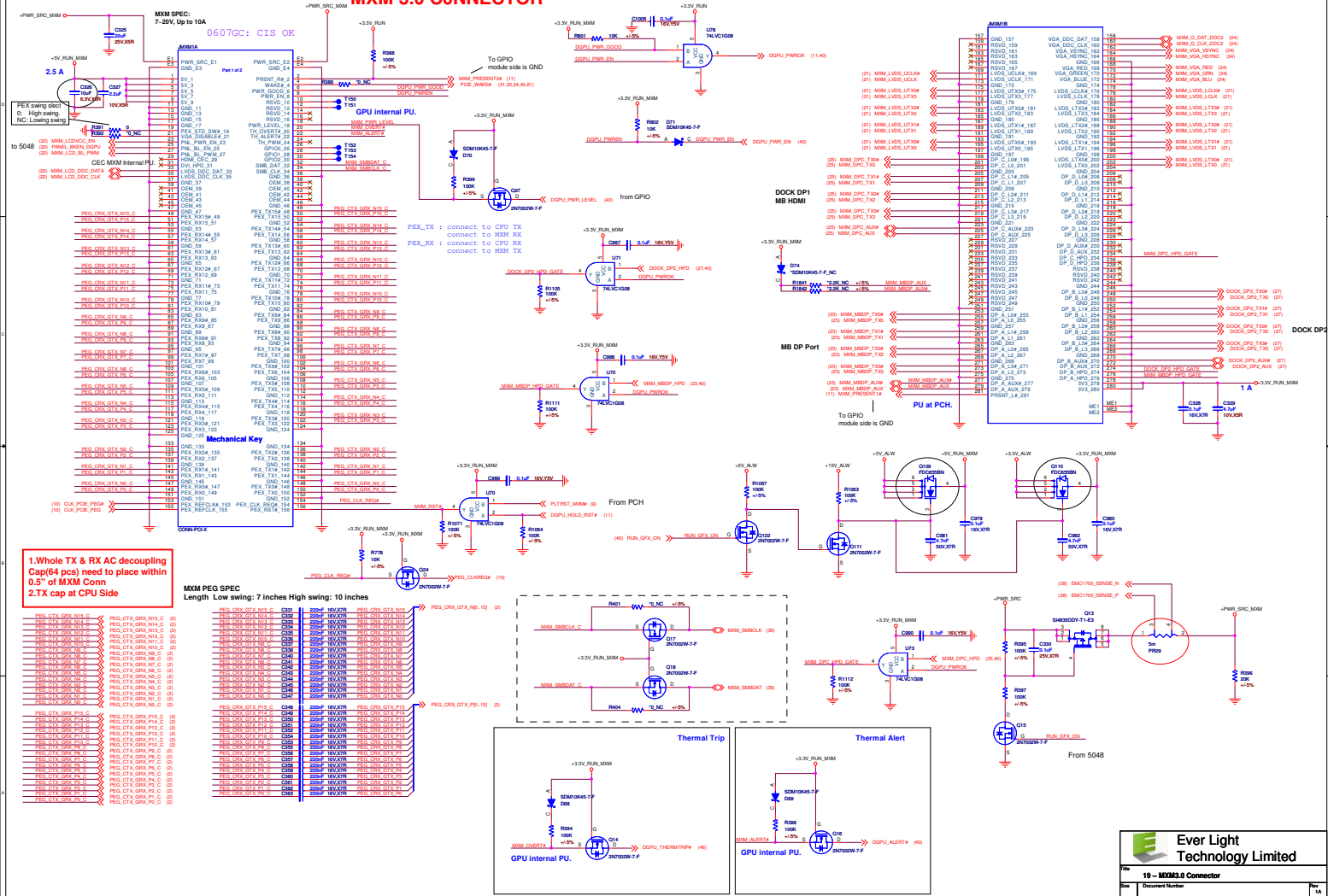
M1: Fixed SO-DIMM VREF_DQ (Default)

M2: Programmable SODIMM VREFDQ



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MXM 3.0 CONNECTOR

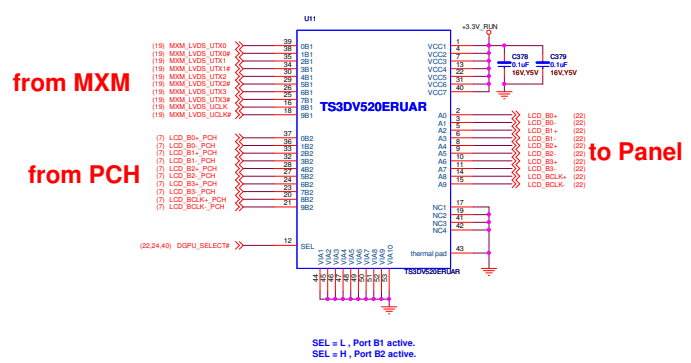
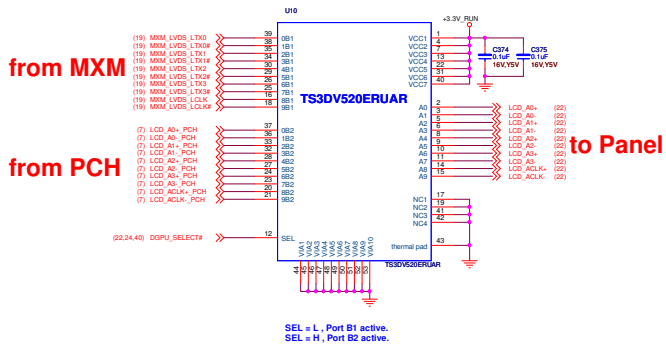


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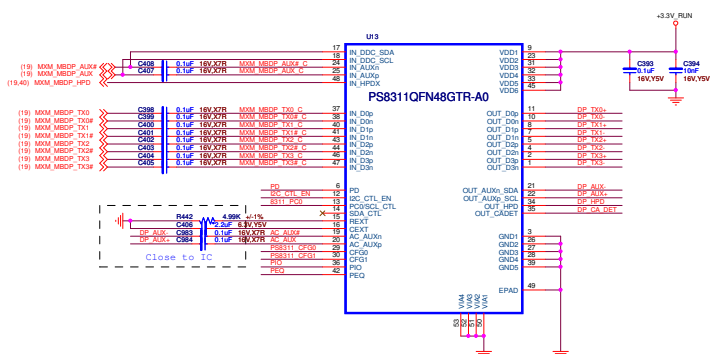
		Ever Light Technology Limited	
File 20 - 17" eDP for PANEL			
Rev	Document Number	Rev	1A
Thunder			
Date: Thursday, January 27, 2011		Sheet	25 of 24

LVDS MUX for Panel



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From dGPU Direct



PC0 : Internal pull down 150k

```
L : automatic equalization enable
H : automatic equalization disable
```

PD : Power down control. Internal

PD : Power down control, Internal pull down 150k

L : Normal operation
H : Chip power down

PIO :

Internal pull down 150k
I. : IN HPD_X=OUT HPD.

```
H : IN_WPDX=OUT_WPD#,
```

13C CTL EN :

Internal pull down 150k

LOW : Pin control
HIGH : I2C control

Chip operation mode, 1

CFG0

L : AUX CH is off when

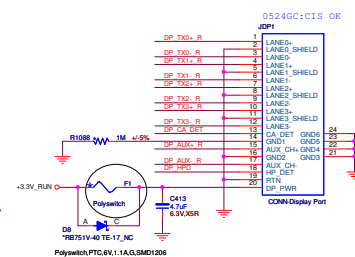
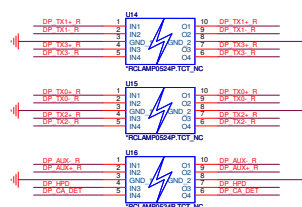
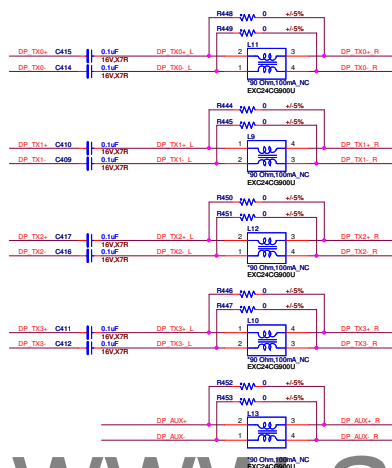
```
H : AUX CH is operative
CFG1
```

L : Normal AUX interface
H : AUX interception

100

PEQ : Programmable input
Internal pull down 150k

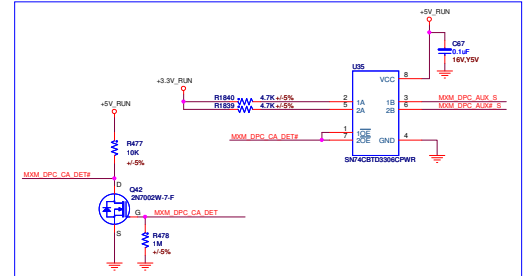
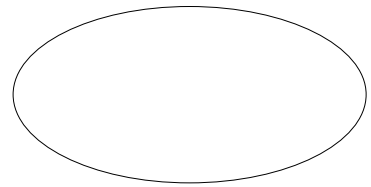
L : Low RX EQ setting
H : High RX EQ setting



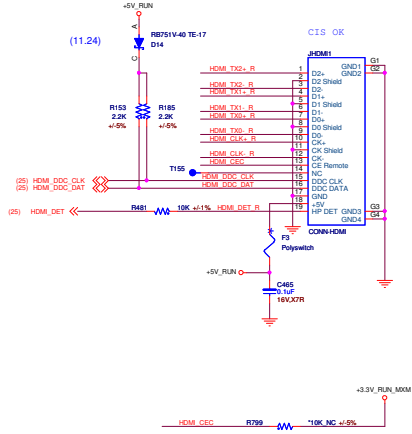
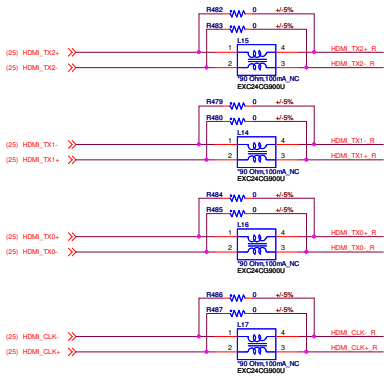
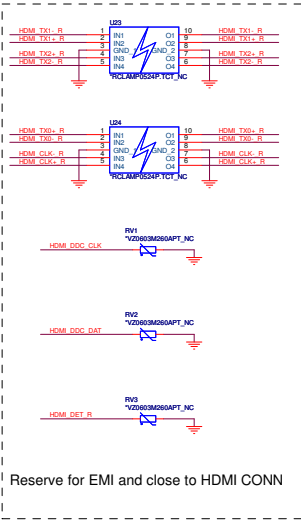
CRT



	A->Port 1	B->Port 1	A->Port 2	B->Port 2
S01/S11 (CRT_SWITCH)	0	0	1	1
S10 (DGPU_SELECT#)	0	1	0	1
S00 (EDID_SELECT#)	0	1	0	1



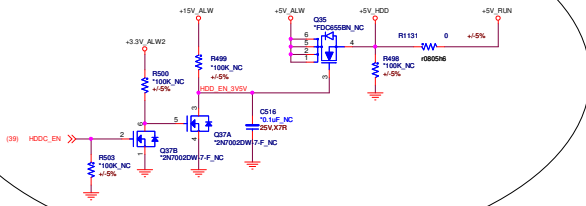
HDMI CONN



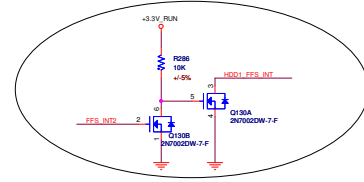
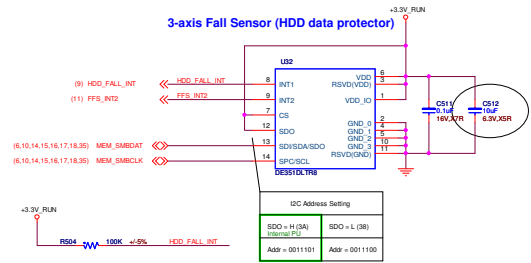
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		Ever Light Technology Limited	
Title		28 - 17" HDD, ODD, G-SENSOR	
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	Thruout		
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HDD POWER

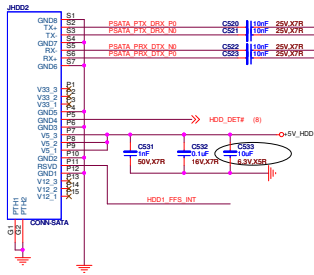


3-axis Fall Sensor (HDD data protector)

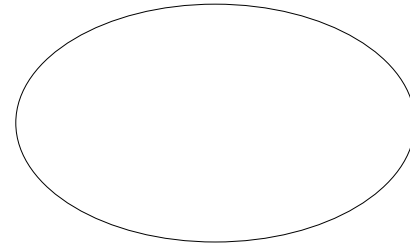


HDD Connector

Main HDD

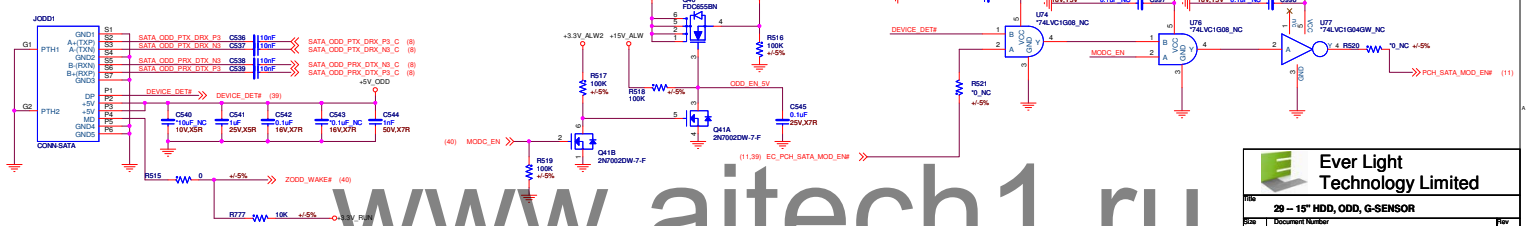


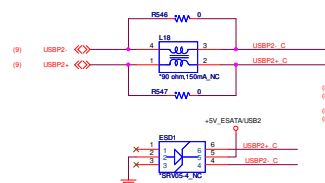
SATA3 Re-Driver For main HDD



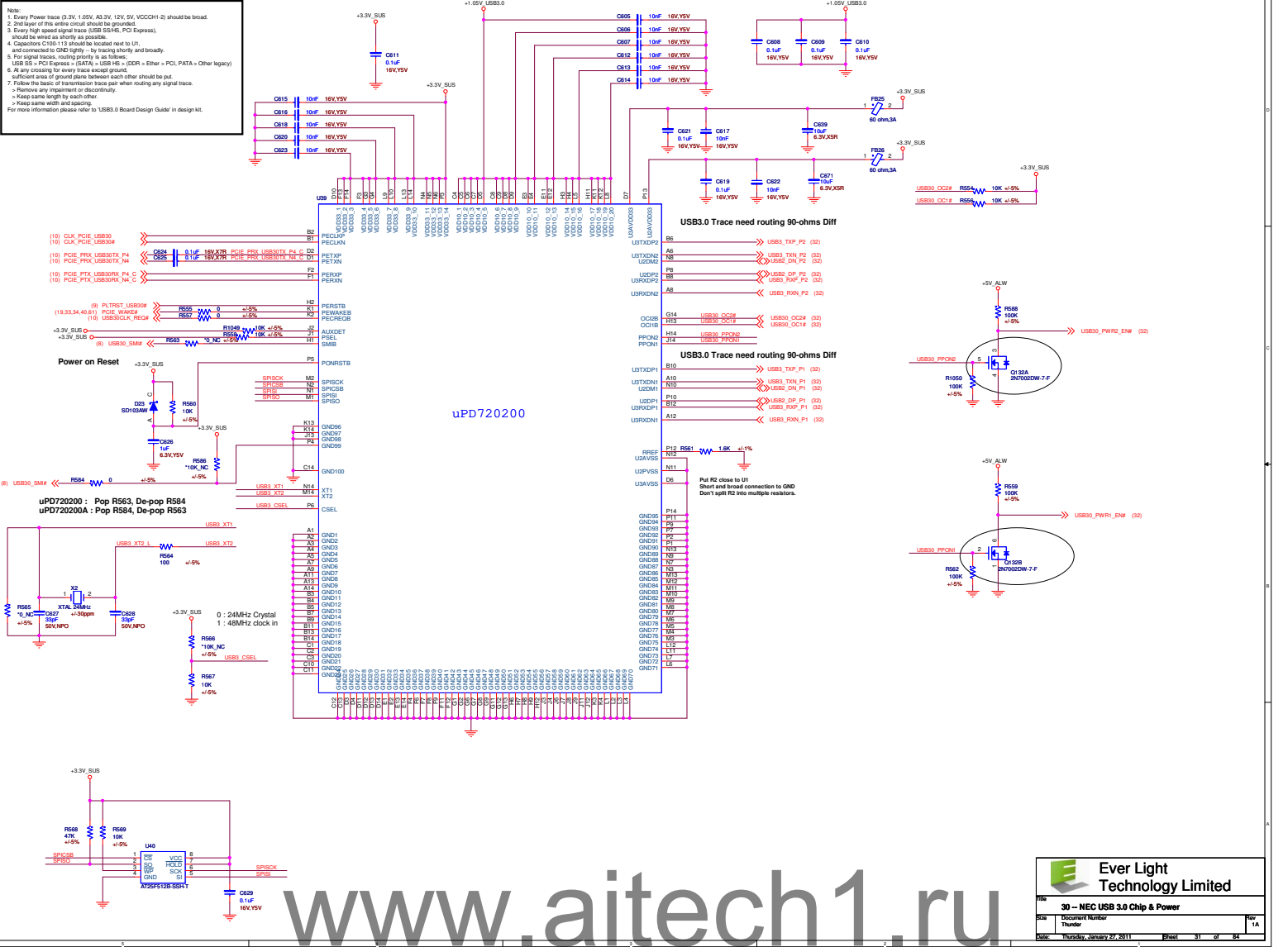
ODD Connector

SATA port 3

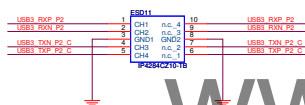
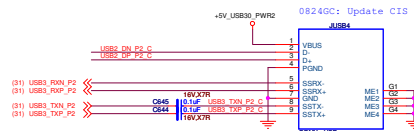
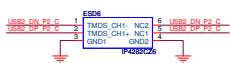
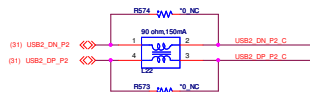
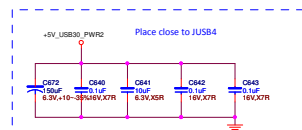
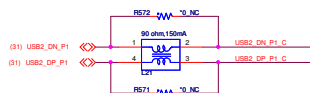
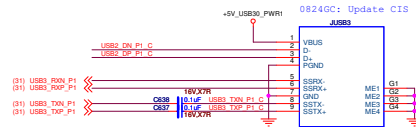
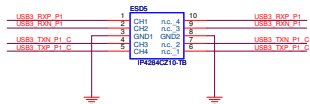
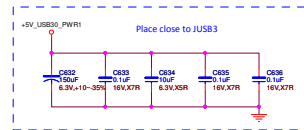
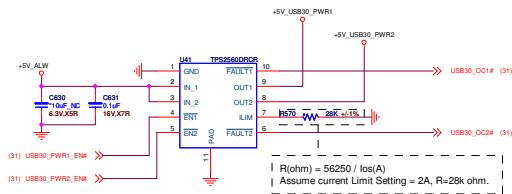


[illegible]

Note:
1. Every Power trace (3.3V, 1.05V, A3.3V, 1.2V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB, SATA, PCI Express), should be routed as short as possible.
4. Capacitors C100-C113 should be located next to U1.
5. For signal traces, routing priority is as follows:
USB SS > PCI Express > SATA > USB HS > (DDR > Ether > PCI, SATA > Other legacy)
6. If any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
8. Remove any impedance or discontinuity.
9. Keep same length to each other.
For more information please refer to USB3.0 Board Design Guide in design kit.

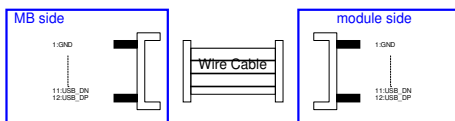
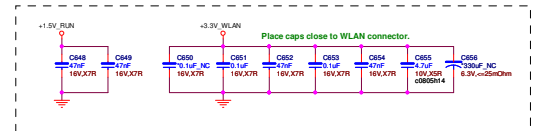
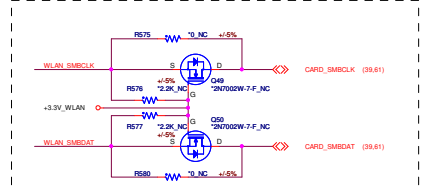


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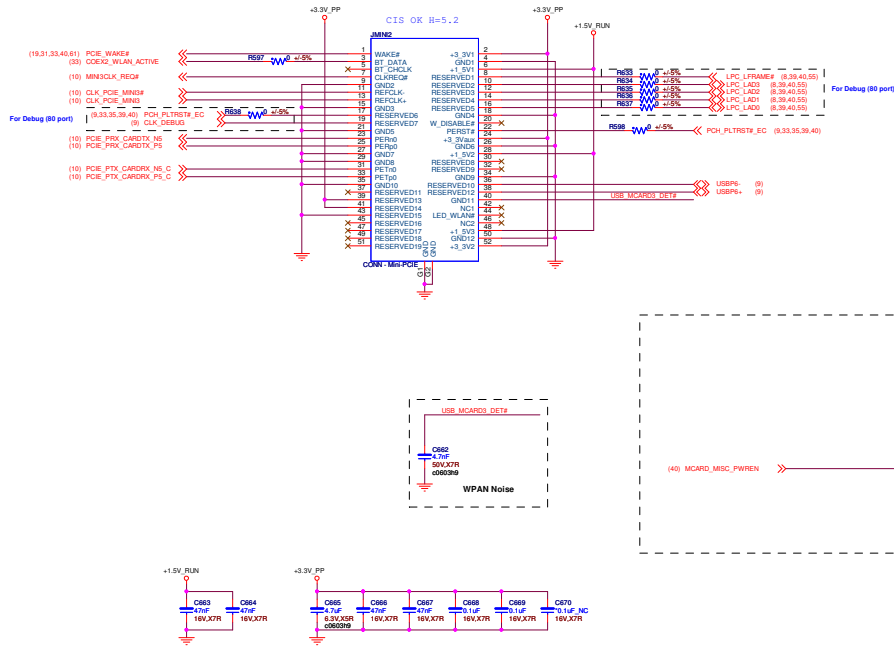


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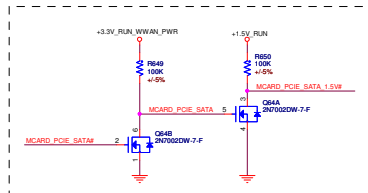
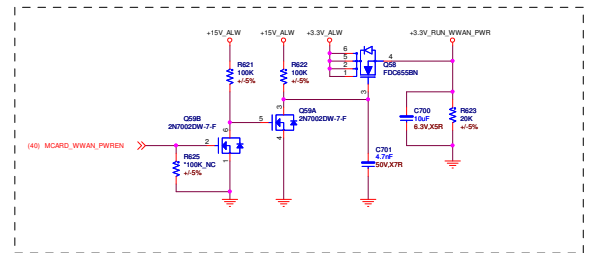
2nd MiniCard connector (WLAN, half size)
MiniCard WLAN connector



3rd MiniCard connector (Flash, half size) MiniCard connector



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[illegible]

0824GC: Update CIS

The diagram shows the 0824GC chip connected to the UIM connector. The UIM connector provides the following signals:

- VIM_PWR**: Connected to the 0824GC VCC pin. A 10uF capacitor is connected to this line to ground.
- UIM_RESET**: Connected to the 0824GC RST pin. A 10k resistor is connected to this line to ground.
- UIM_CLK**: Connected to the 0824GC CLK pin.
- UIM_VPP**: Connected to the 0824GC VPP pin.
- UIM_DATA**: Connected to the 0824GC C7 pin. A 10k resistor is connected to this line to ground.
- UIM_GND**: Connected to the 0824GC GND pins.

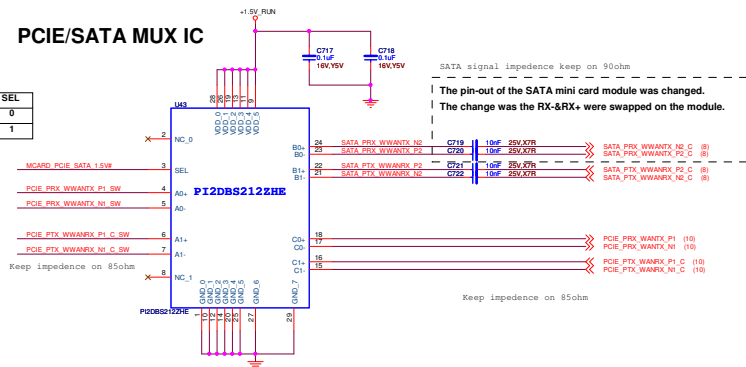
The 0824GC chip has the following pins:

- VCC**: Connected to VIM_PWR.
- GND**: Connected to UIM_GND.
- CS**: Connected to UIM_VPP.
- RST**: Connected to UIM_RESET.
- VPP**: Connected to UIM_VPP.
- C7**: Connected to UIM_DATA.
- CLK**: Connected to UIM_CLK.
- GND**: Connected to UIM_GND.

Place UIM_PWR cap close to SIM card connect.

Place as close as possible to J1M1 connector

Function	SEL
Port A to Port B	0
Port A to Port C	1



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-1%	1000	750	
	+/-1%	330	200	250 (max; constant) 5 (Not recommended)
+1.5V	+/-1%	500	350	NA

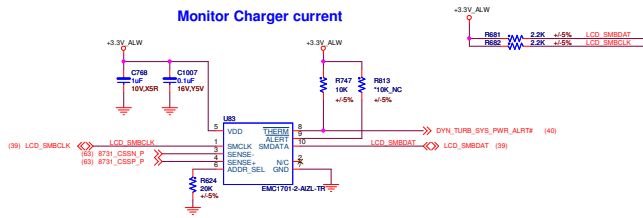
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		Ever Light Technology Limited	
File 36 - 17" WWANL SM			
Rev	Document Number		Rev 1A
Date Thursday, January 27, 2011		Sheet	36 of 84

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		Ever Light Technology Limited	
File 37 - 17" NVRAM-MUX			
Size	Document Number	Rev	
	Thunder	1A	
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Monitor Charger current

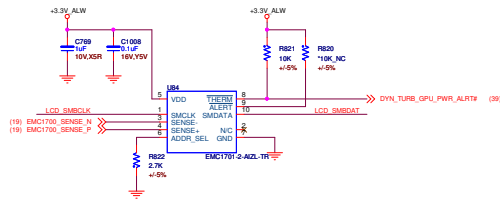


RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)	1600	0101_000(r/w)
100	1001_101(r/w)	2000	0101_001(r/w)
180	1001_110(r/w)	2700	0101_010(r/w)
300	1001_111(r/w)	3600	0101_011(r/w)
430	1001_000(r/w)	5600	0101_100(r/w)
560	1001_001(r/w)	9100	0101_100(r/w)
750	1001_010(r/w)	20000	0101_101(r/w)
1270	1001_011(r/w)	Open	0111_000(r/w)

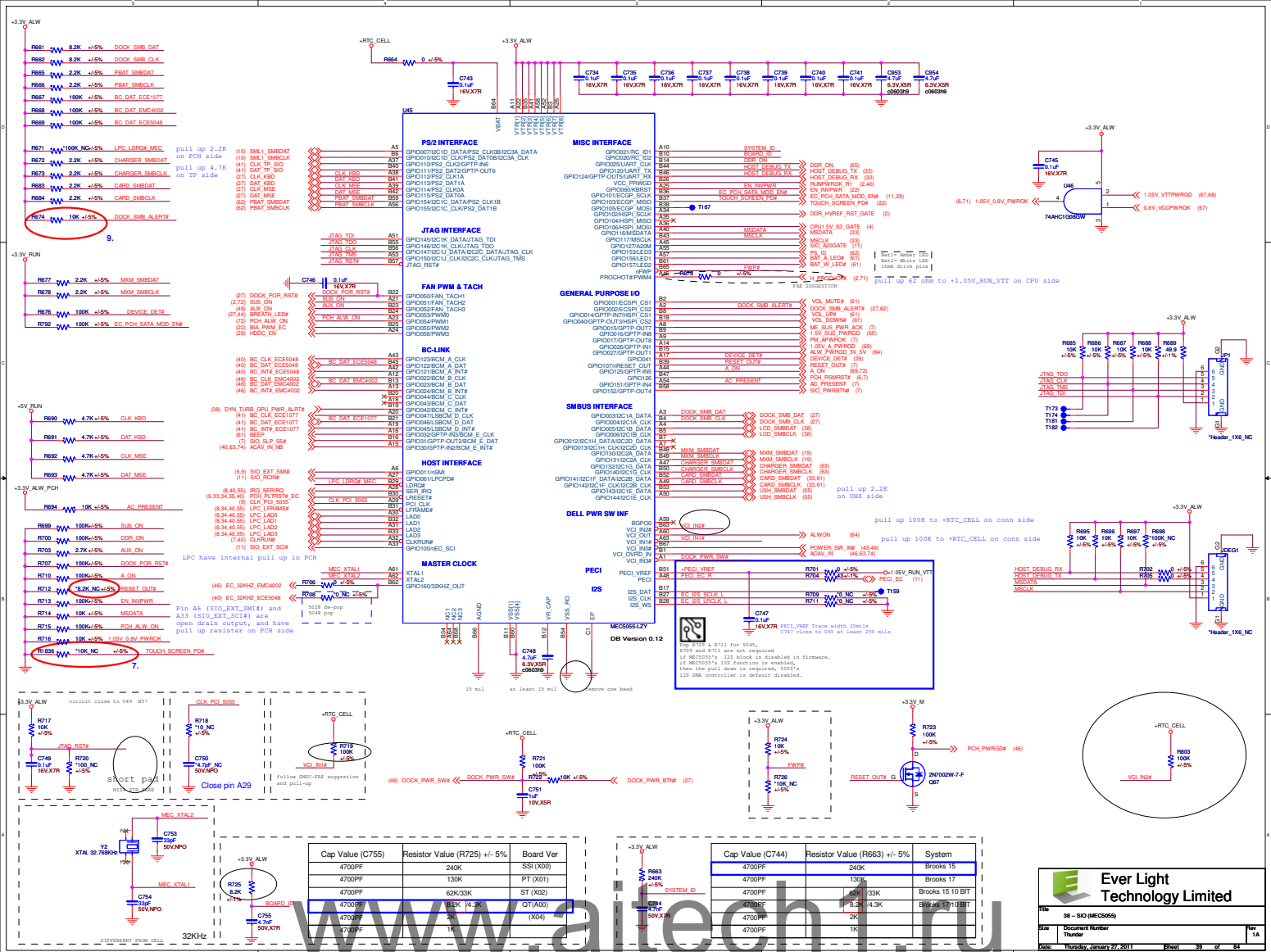
U84

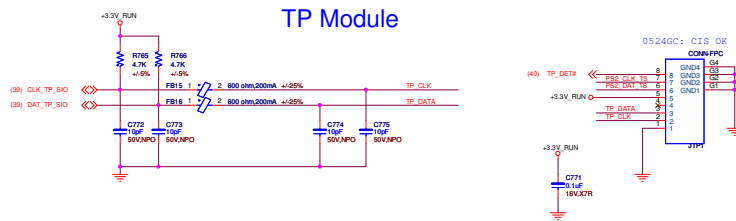
U83

Monitor PWR_SRC_MXM

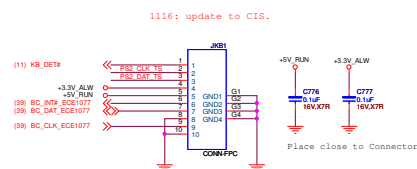


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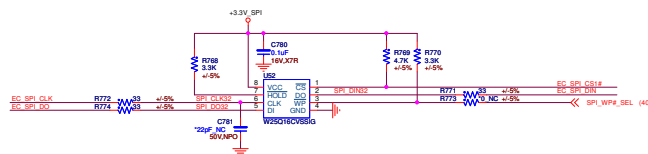


Keyboard Module

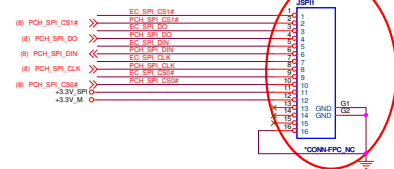
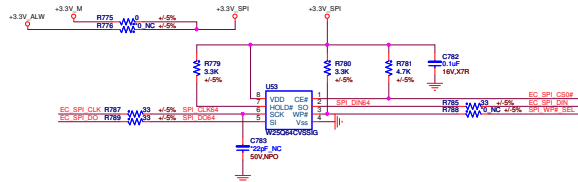


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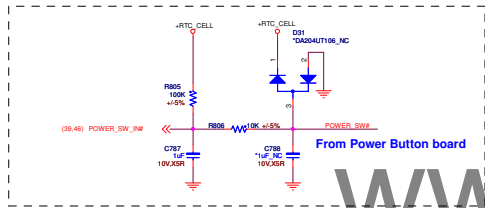
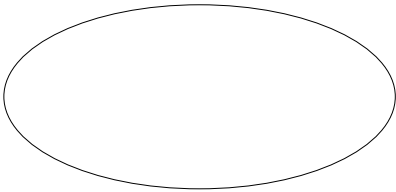
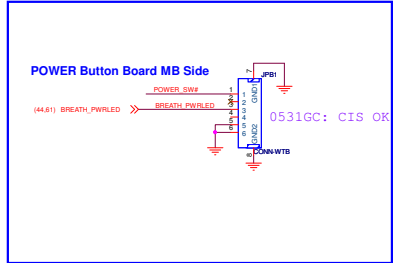
PCH, EC SPI ROM For BIOS (2M Byte)



PCH SPI ROM For iAMT (8M Byte)



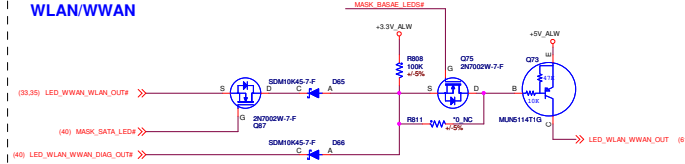
Put close to JSPH



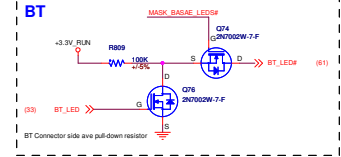
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Ever Light Technology Limited	
43 - DB Connector x 7	
Date: Thursday, January 27, 2011	Rev: 1A

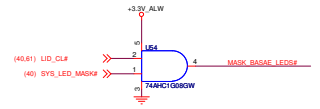
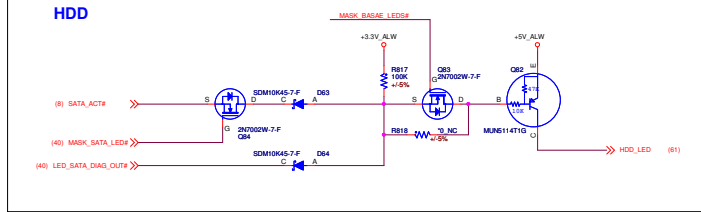
WLAN/WWAN



BT



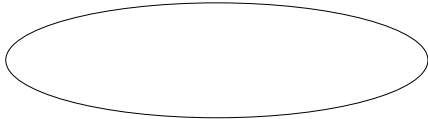
HDD



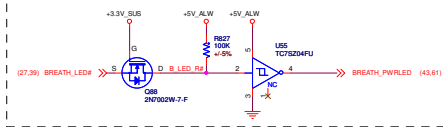
Charge

White

Amber

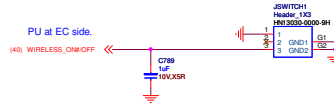


BREATH PWRLED



From TOP View:

↑ WIRELESS_OFF
↓ WIRELESS_ON



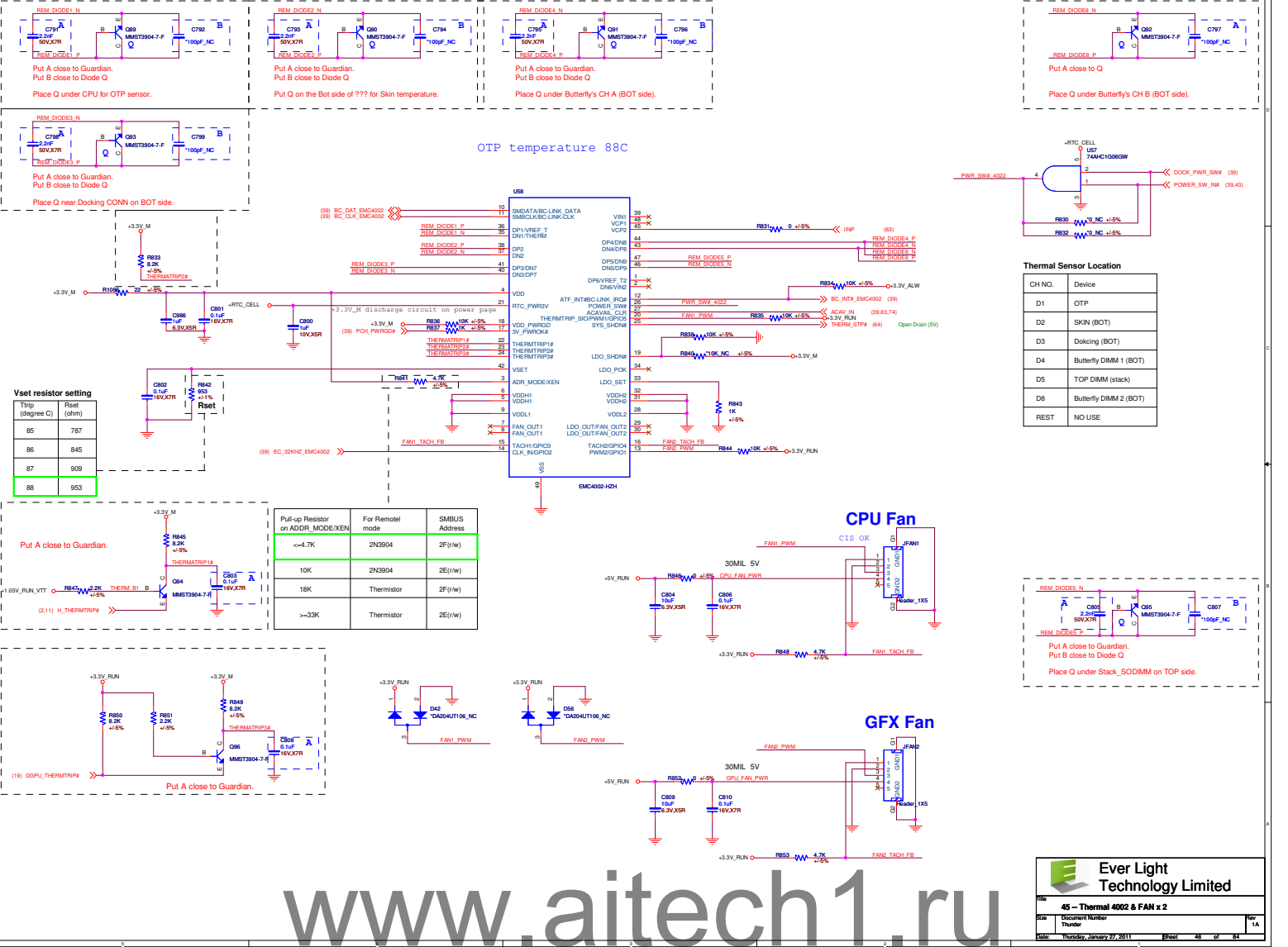
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44 - LED+Control, Wirele	
File 44 - LED+Control, Wirele	Rev 1A
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Remove IOL Board


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		Ever Light Technology Limited	
File		45 - Hall sensor	
Rev	Document Number		
	Revised		
Date		Thursday, January 27, 2011	Sheet 45 of 84




Move to IOL board

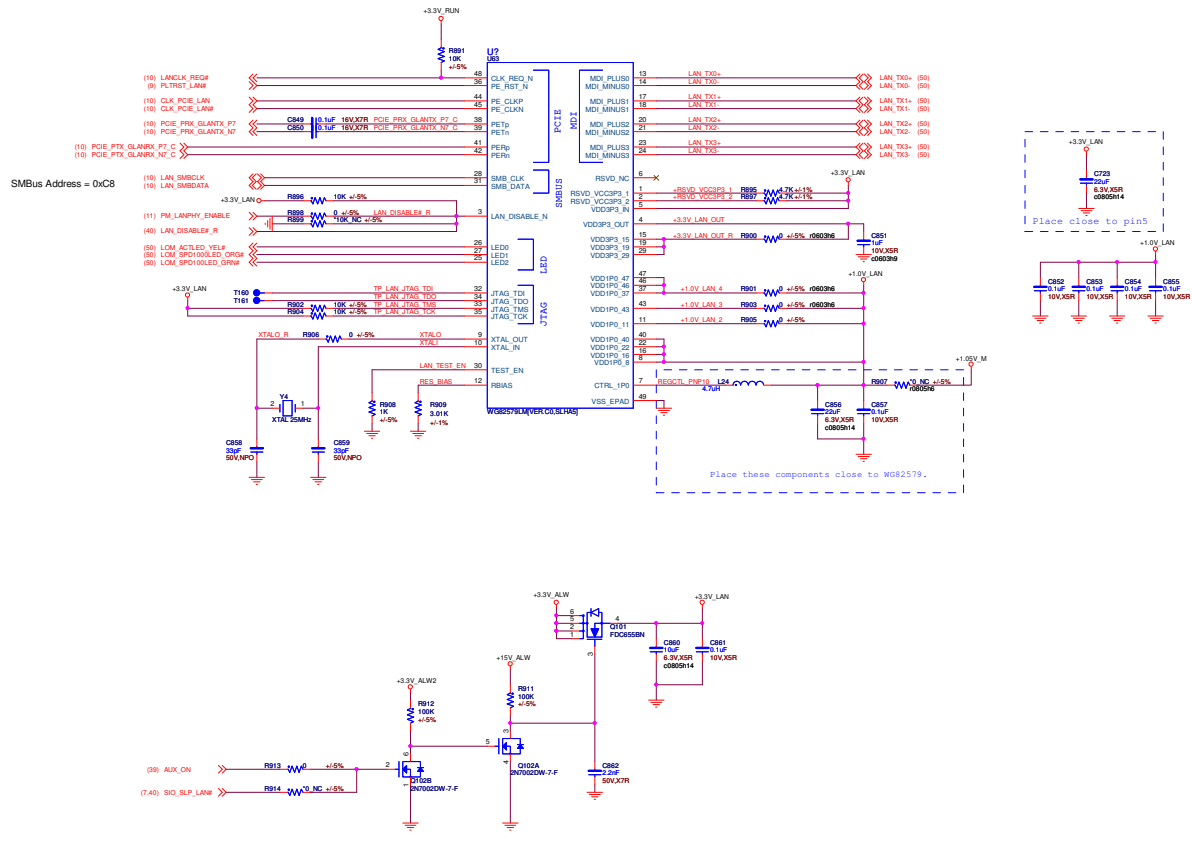
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		Ever Light Technology Limited	
File 47 - AUDIO(92HD80B)+SPK+JACK			
Size	Document Number	Rev	
	Thunder	1A	
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Move to IOL board

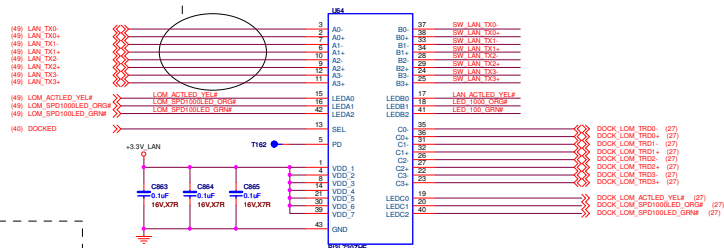
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		Ever Light Technology Limited	
File		48 -- AUDIO for Docking+Crystal	
Rev	Document Number		
	Thruout		
Date		Thursday, January 27, 2011	Sheet 48 of 84



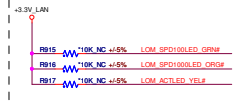
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No need for Intel LAN.



DOCKED
SEL 0: RJ45,
SEL 1: Dock.

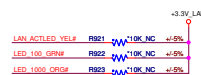
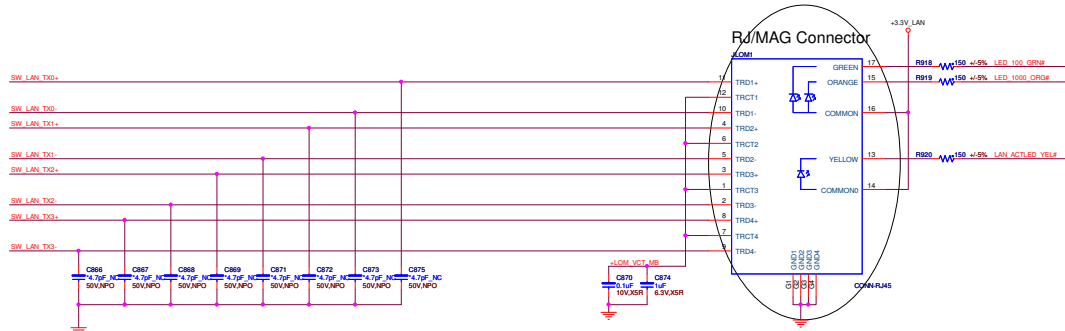
Reserve pull up.



LAN Switch table

DOCKED(SEL)	LOM signals	LED SIGNALS	Switch
L	Ax to Bx	LED Ax to LED Bx	MB
H	Ax to Cx	LED Ax to LED Cx	DOCK

Need to update connector PN.




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		Ever Light Technology Limited	
File 50 - TPM for China			
Rev	Document Number	Rev	1A
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Move to IOL board

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		Ever Light Technology Limited	
File S1 - Card Reader & Conn			
Rev	Document Number	Rev	1A
	Thunder		
Date	Thursday, January 27, 2011	Sheet	55 of 84

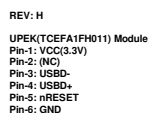
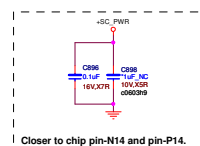
Move to IOL board

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		Ever Light Technology Limited	
File 52 - 15" 1394 Conn			
Rev	Document Number	Rev	
	42600	1A	
Date: Thursday, January 27, 2011		Sheet	55 of 84

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		Ever Light Technology Limited	
File: 53 - 17" 1394 Conn+ Power			
Rev	Document Number	Rev	1A
	Thunder		
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ST_M45PE16-VMW6TG
ATMEI AT45DB161D-SII-SI 955



Move to IOL board

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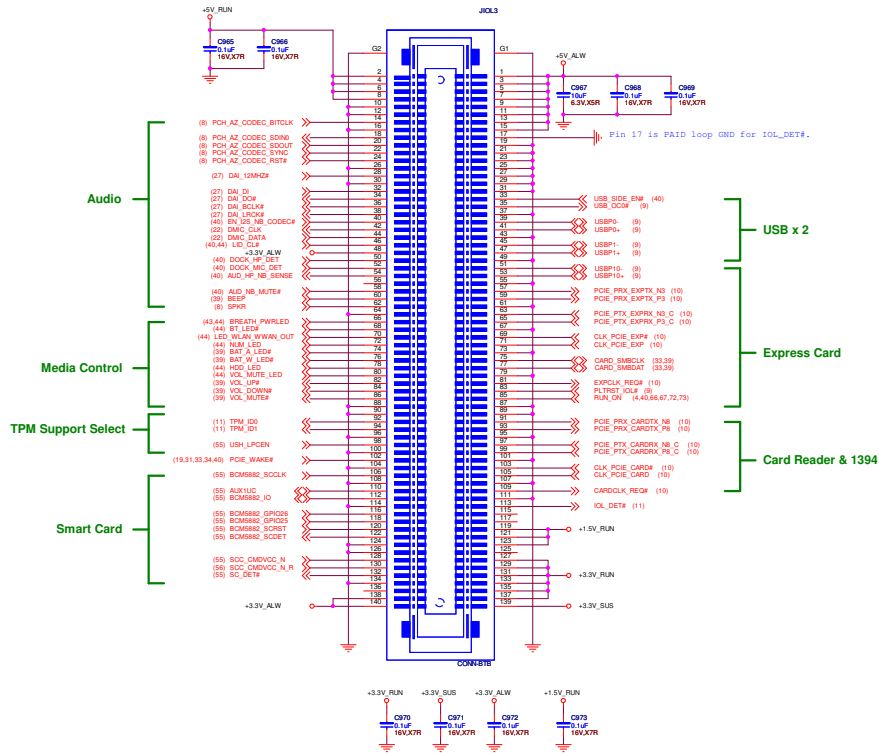
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Size: Document Number		Rev: 1A	
Date: Thursday, January 27, 2011		Sheet: 55 of 84	



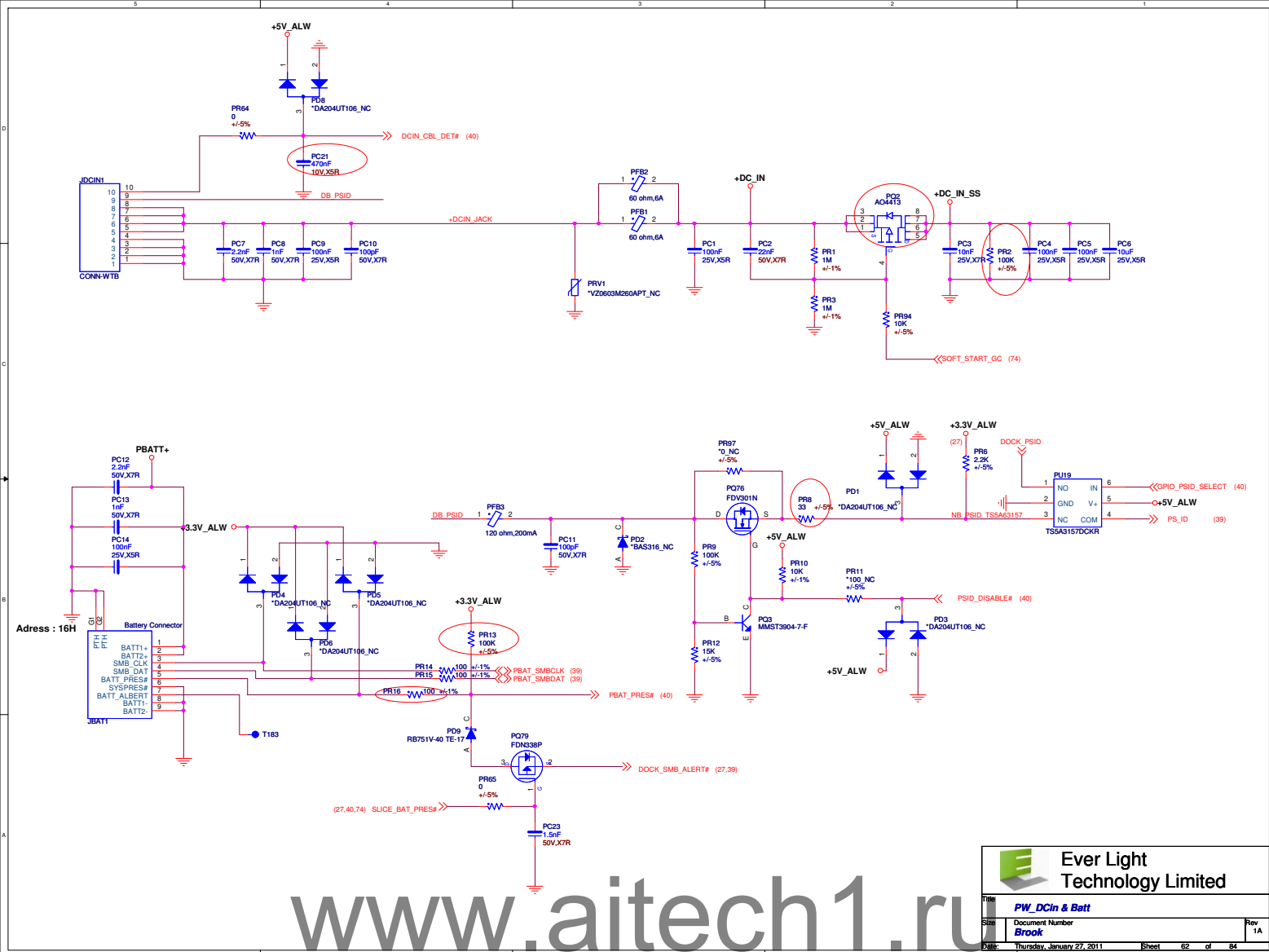
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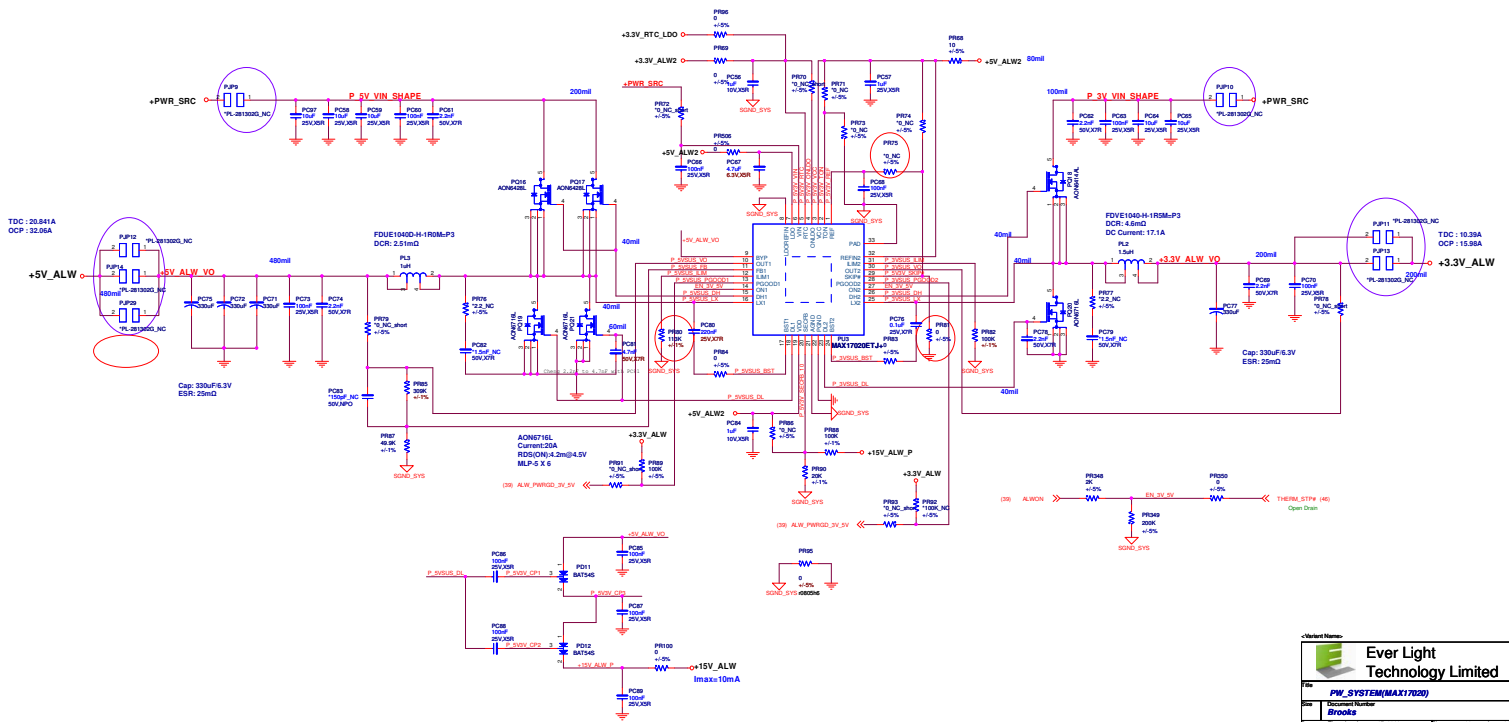
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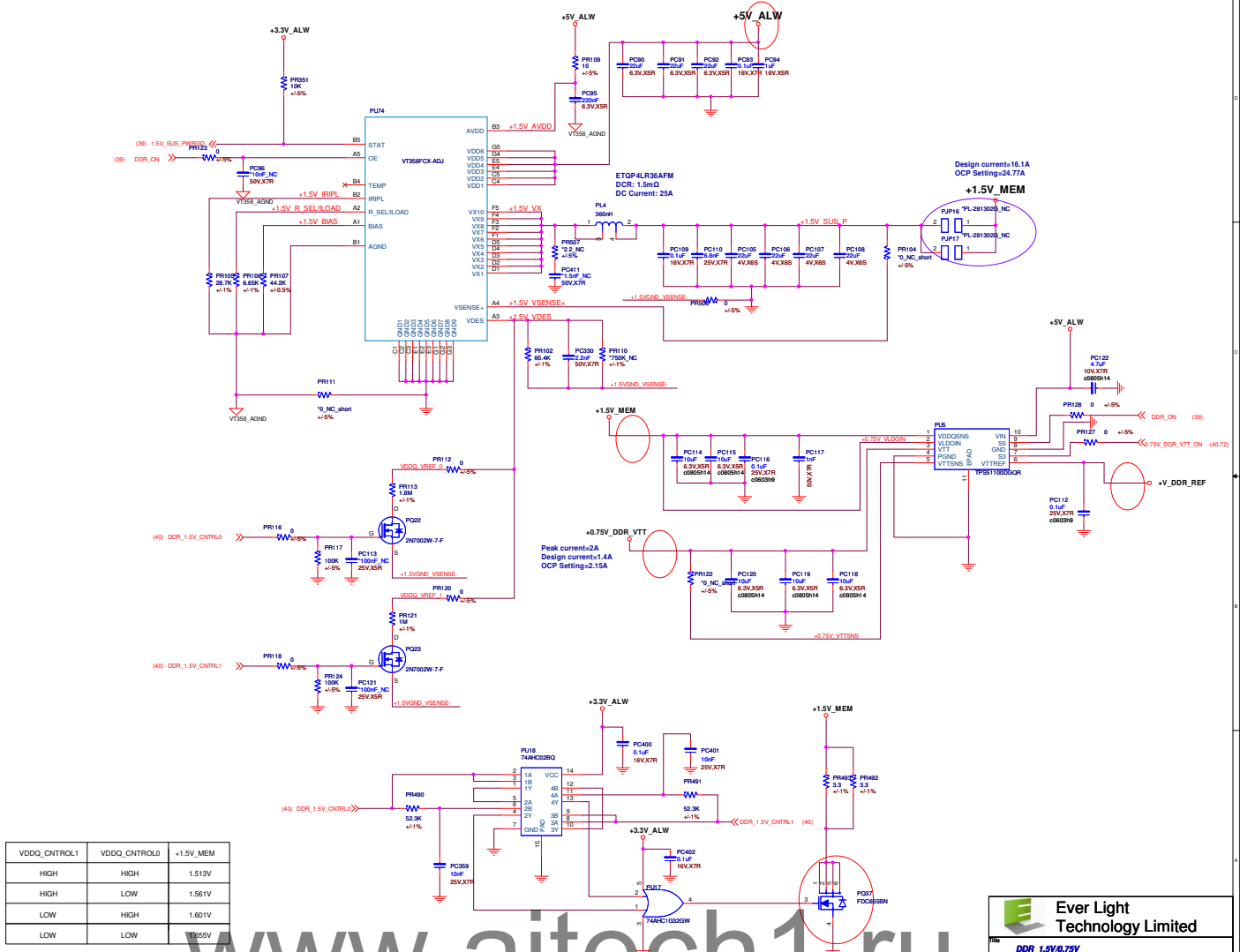
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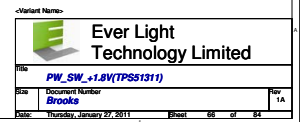


+5V_ALW / +3.3V_ALW POWER SUPPLY

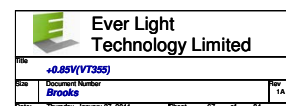


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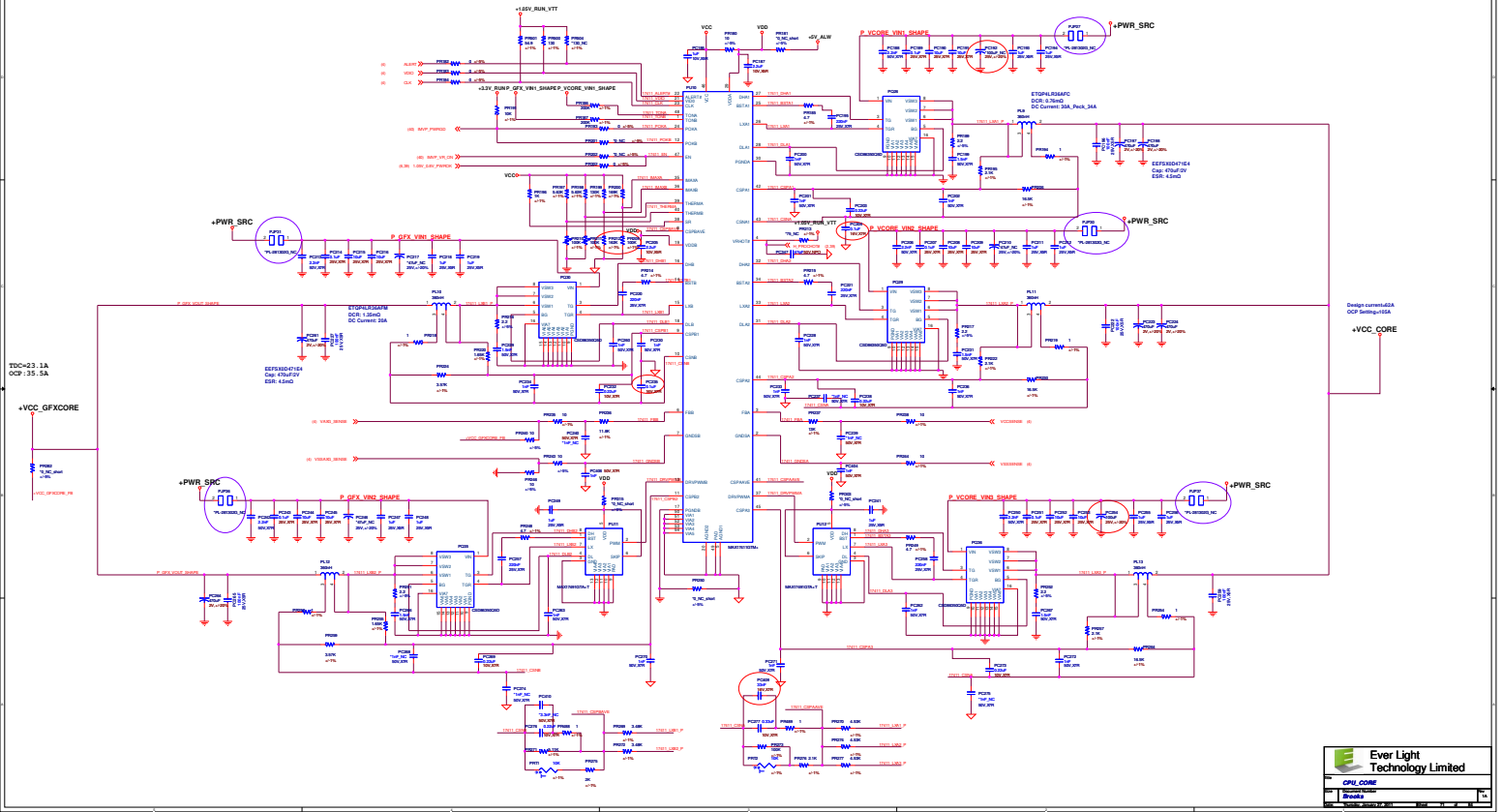


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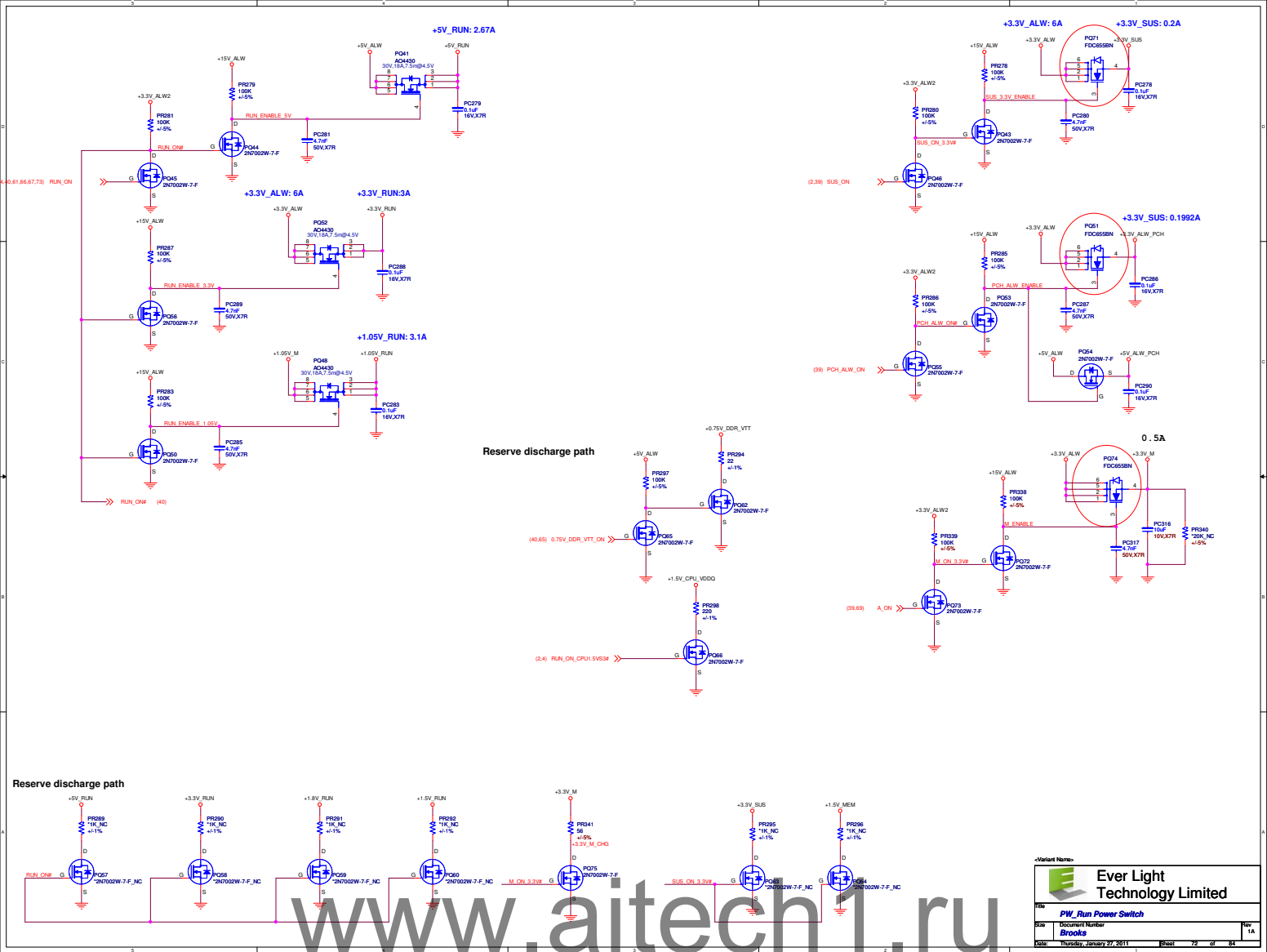


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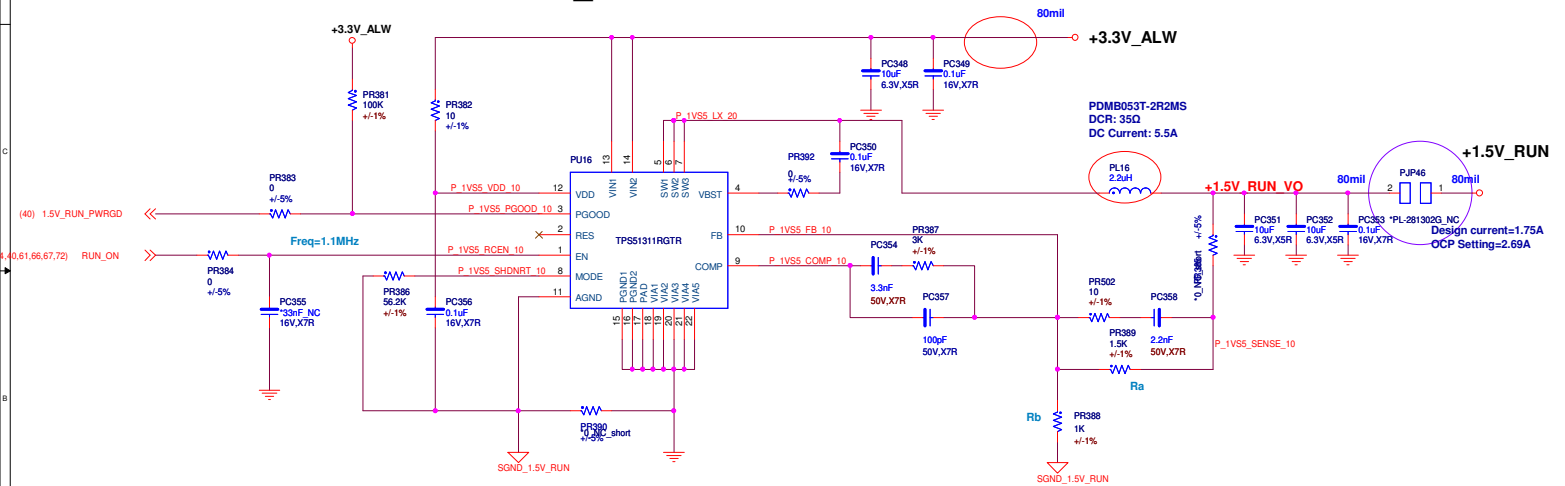
IMPV7 CPU/GPU VCORE REGULATOR



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+1.5V_RUN POWER SUPPLY



<Variant Name>



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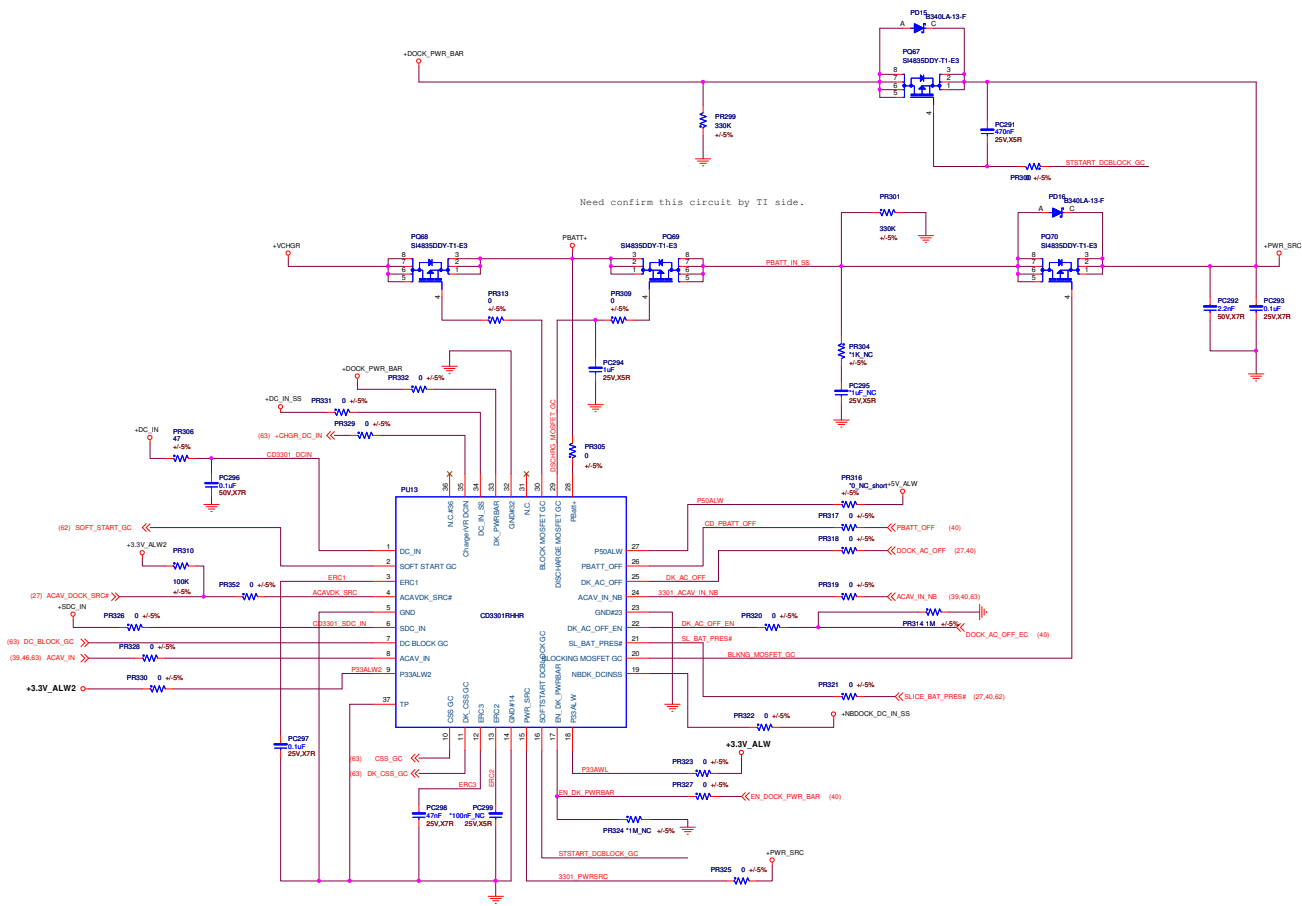
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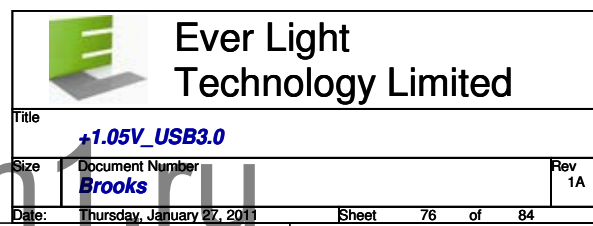
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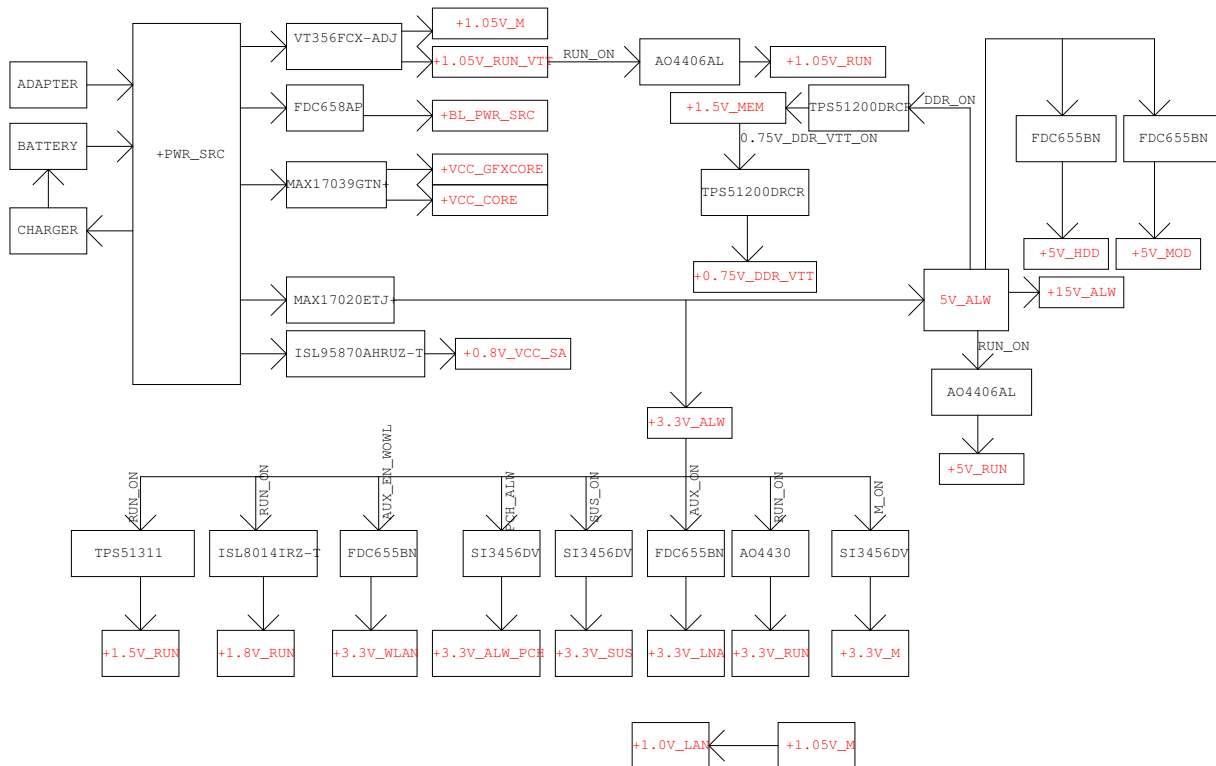


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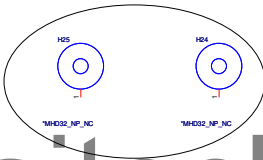
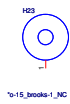
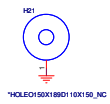
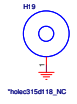
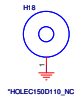
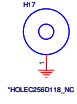
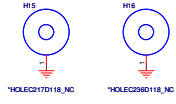
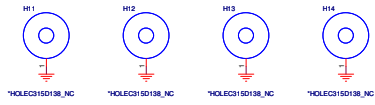
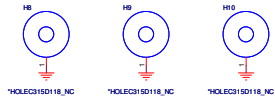
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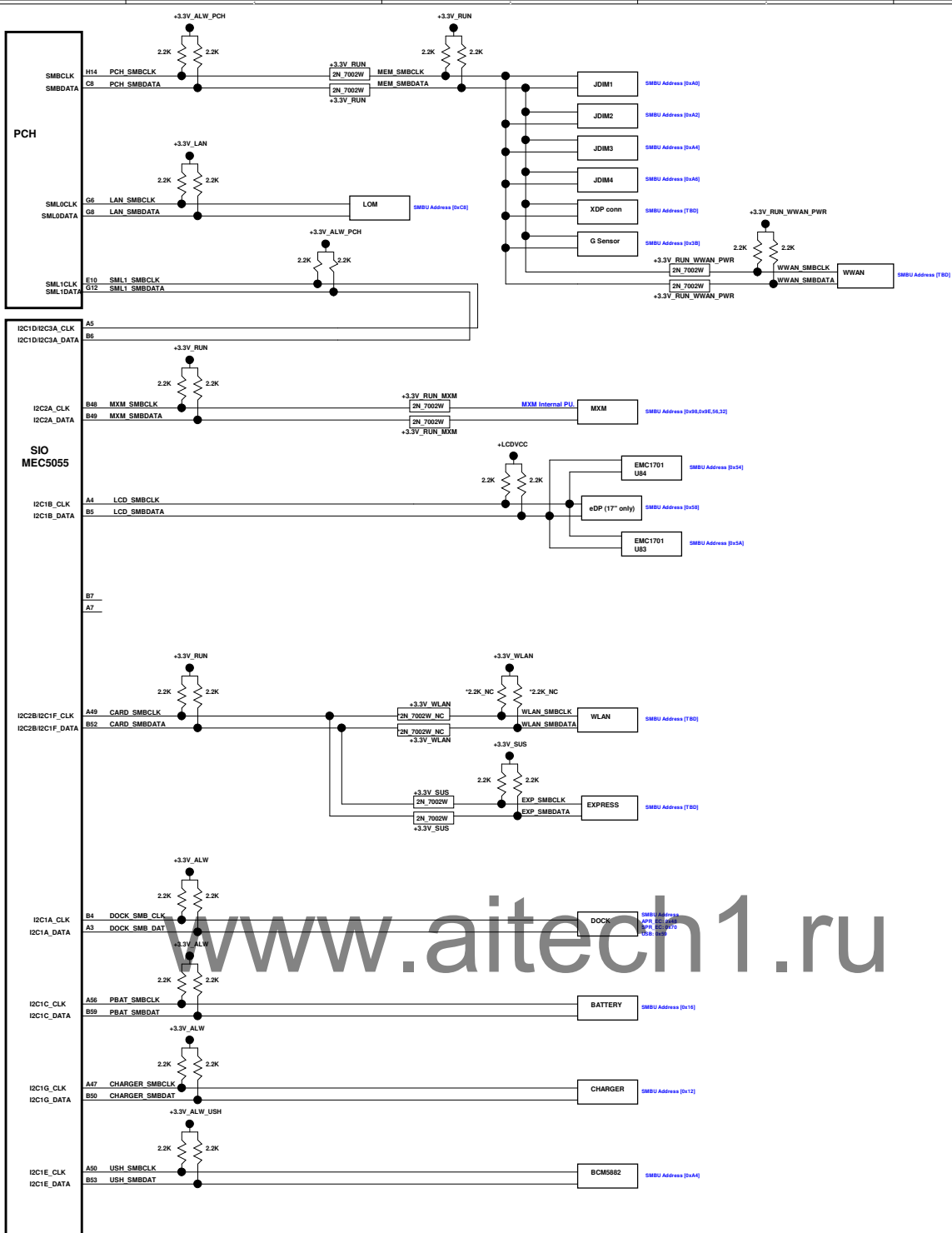


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71 - PAD,SCREW & Sitching CAPs		
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Title 73 – Power Sequence Diagram			
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Title			
74 - Power Sequence Timing			
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Change List

Item	Date	Page#	Issue Description
			A00
1.	0112	02	Per Intel DG, eDP_HPD can be NC. NC R57.
2.	0112	02	R39 change from 5.1K to 4.99K.
3.	0112	39	Per Macallan sch, RESET_OUT# PD 8.2K is no necessary. NC R712.
4.	0112	42	JSP11 NC.
5.	0112	9	PCI_REQ2# PU resistor change from 100K to 10K.
6.	0112	12	Per Intel DG, +PCH_V5REF_SUS C184 change from 1uF to 0.1uF.
7.	0112	39	TOUCH_SCREEN_PD# PD resistor is not necessary. NC R1836.
8.	0112	40	DCIN_CBL_DEV# PU resistor change from 10K to 100K.
9.	0112	39	DOCK_SMB_ALERT# PU resistor change from 100K to 10K.
10.	0117	55-57	Update Broadcom 5882 PN from BCM58821B0KFBG to BCM5882B0KFBG.
11.	0117	27	Change C499 to ESD12 and delete C500. adding ESD13 at DOCK_RST_R# and update to CIS part.
12.	0117	39	Update board ID to A00.
13.	0117	44	Remove volume mute LED. NC Q81.
14.	0117	23	Change F1 from fuse (2411) to Polyswitch type (1206).
15.	0117	23	Adding two NPTH screw hole (MHD32_NP)
16.	0117	22	Populate camera USB common mode choke.
17.	0120	11	Update PCH GPIO28 circuit, delete C36 and connect SLP_ME_CSW_DEV# to PCH GPIO28 directly. Adding 4.7K PU to +3.3V_ALW_PCH.
18.	0120	39	Update board ID value to 8.2K.
19.	0120	25	Brooks 15 change R470 from 5.11k ohms to 5.49k ohms, Brooks 17 change R1927 from 5.11k ohms to 5.6k ohms
20.	0127		Update PCH and LOM PN. 5055 new PN has no available and change to TBD.

PROJECT: T1000V

DOC: NC-XXXX

REV: XXX

APPROVED BY: (Signature)

CHECKED BY: (Signature)

DRAWN BY: (Signature)

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75 - Change List

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POWER SATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0(Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (Soft off) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3(Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (Soft off) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

Power Plane \ State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	Right Side top
	1	Right Side bot
	2	Back Side
	3	NC
	4	2nd Mini Card (WLAN/WIMAX)
	5	1st Mini Card (WWAN)
	6	3rd Mini Card
	7	USH
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	BlueTooth
	12	Camera
	13	LCD Touch or Nvidia 3D IR
USH	0	BIO
	1	NC

PCH	PCI EXPRESS	DESTINATION
	Lane 1	1st Mini Card WWAN
	Lane 2	2nd Mini Card WLAN
	Lane 3	Express Card
	Lane 4	USB 3.0
	Lane 5	3rd Mini-Card
	Lane 6	4th Mini-Card
	Lane 7	LAN
	Lane 8	Card Reader

PCH	SATA	DESTINATION
	SATA 0	HDD 1st
	SATA 1	HDD 2nd
	SATA 2	MINI CARD
	SATA 3	ODD
	SATA 4	E-SATA
	SATA 5	Docking

MXM Graphics Module	MXM PORT	CONNECTION
	PORT A	MB DP Port
	PORT B	DOCK DP2
	PORT C	DOCK DP1 and MB HDMI
	PORT D	eDP Panel

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Change List

Item	Date	Page#	Issue Description
			ST2_power
1.	1229	62	PR2 change from 10K to 100K for E3 leverage
2	1229	64	Change to skip mode; PR75 to NC, PR81 to stuff
3	1230	63	PR58 footprint change from r2512_1h7 to r2512_1h7_mik
4	1231	63	PD17 no stuff
			A00_power
5	0117	62	PR13 change from 10K to 100K
6	0117	62	PR8 change from 100 to 33 (change from 0603 10 0402)
7	0117	62	PR8 change from 100 to 33
8	0117	63	PC24 stuff to follow on E3
9	0117		Upsale total 23 jumps
10	0118	62	PR16 move to front of battery connector.
11	0125	63	PC24 no stuff.
12	0125	62	PC21 stuff.
13	0126	71	AL cap change from FC192 to PC254. FC192 no stuff for temp.